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S1D13521B01 Epson / E Ink Broadsheet

Hardware Functional Specification

SEIKO EPSON CORPORATION

Rev. 1.2

NOTICE

Table Of Contents

Chapter 1 Introduction

1.1 Scope

This is the Hardware Functional Specification for the S1D13521B01 EPD Controller. Included in this document are timing diagrams, AC and DC characteristics, register descriptions, and power management descriptions. This document is intended for two audiences: Display Subsystem Designers and Software Developers.

This document is updated as appropriate. Please check for the latest revision of this document before beginning any development. The latest revision can be downloaded at www.erd.epson.com.

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1.2 Overview Description

EPSON's S1D13521 controller provides a high performance, low cost, solution for current and future E Ink EPDs (Electronic Paper Displays). The controller greatly reduces CPU overhead by providing many functions that were previously handled by the Host.

S1D13521 allows multi-regional and concurrent display updates resulting in highly responsive screen changes. This increased responsiveness finally makes touch pen support and on-screen user interfaces viable, opening up a range of new applications.

Additionally, the S1D13521 integrates support for current and future power management chips, as well as future 16 and 32 gray level waveforms. All this is achieved with a lower parts cost than previous EPD controllers making the S1D13521 a perfect choice for new designs and design upgrades.

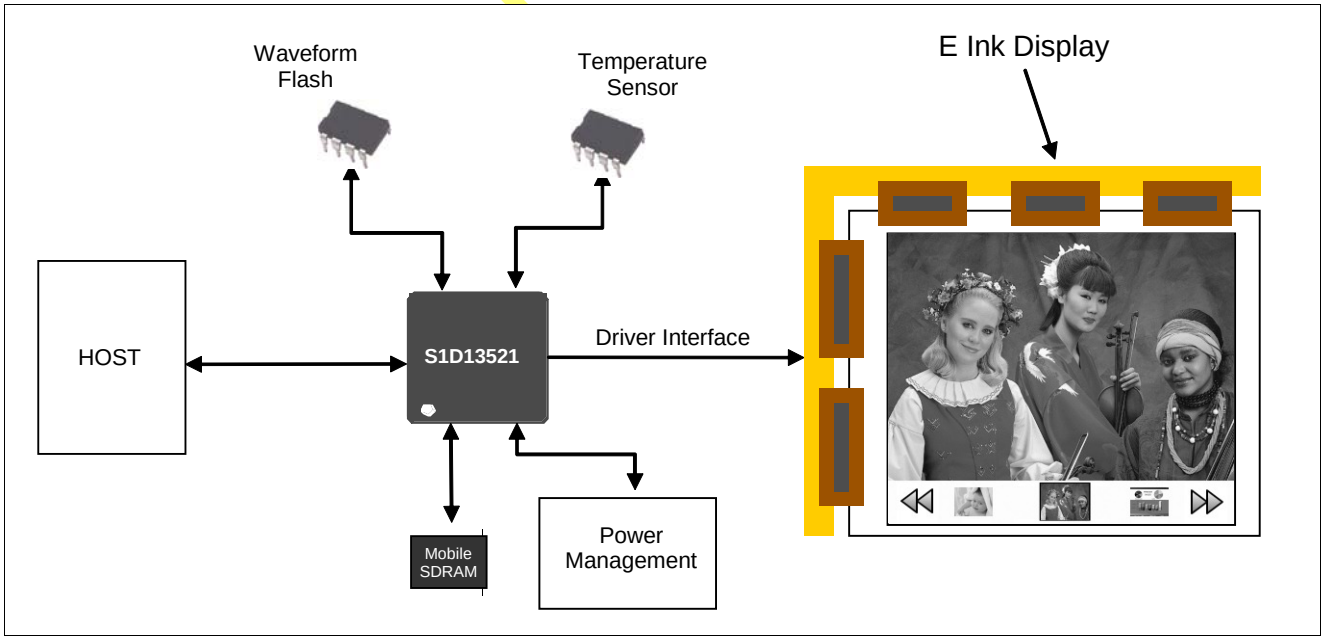


Figure 1-1: S1D13521 Overview

Chapter 2 Features

2.1 Direct Source and Gate Driver for Electrophoretic Display

- Supports up to 2048x1536 resolution @ 50Hz
- Supports up to 4096x4096 resolution @ less than 50Hz (see 10.7, “Resolution Support” on page 93)
- Up to 5-bit grayscale waveforms (2 / 3 / 4 / 5 bpp)
- Source Driver interfaces to the Micronix MX860 IC and compatible devices
  - Programmable up to 1024 pixels per IC
- Gate Driver interfaces to the Sharp LH1692 and compatible devices
- Panel Border Support

2.2 16-Bit Host Interface

- Indirect 16-bit Host Bus Interface (Intel 80)
- Registers can be accessed using Command Mode
- User programmed commands can be used to execute a pre-programmed series of commands
- DMA compatible memory bus style host interface

2.3 External Memory SDRAM Interface

- 16/32-bit mobile SDRAM Interface
- Programmable Column Addressing Width
- Maximum operating frequency: 133MHz

2.4 Power Management IC Support

- Supports 3-wire Active Matrix Power Management ICs

2.5 Image Buffer Flexibility

- Host Writes can be rotated counter-clockwise by 90°, 180°, or 270°
- Host Write data input can use packed mode for high-speed transfers
- New image data can be loaded to the image buffer while display updates are in progress

2.6 I2C Thermal Sensor Temperature Reading

- Supports I2C sequence for temperature reading
- Supports National LM75 Digital Temperature Sensor and compatible devices

2.7 Serial Flash Memory Waveform Read

- Serial Flash Memory for Waveform Reads
- High Speed SPI Mode (the Fast Read command must be supported by the Flash Memory)
- Waveform format: E Ink's waveform version 1 and version 2 (voltage controlled waveform)

2.8 Clock Source

- Internal Programmable PLL
- Single clock input: CLKI
- Two terminal Crystal interface: OSCI/OSCO

2.9 Miscellaneous

- Sleep and Standby Power Save Modes
- General Purpose Input/Output pins are available (GPIO[1:0])
  - Interrupt pin associated with selectable GPIO inputs
- Packages:
  - PFBGA8UX 181-pin (8mm x 8mm x 1.2mm, 0.5mm ball pitch)
  - PFBGA12UX 180-pin (12mm x 12mm x 1.2mm, 0.8mm ball pitch)
- Core Voltage: 1.8V
- IO Voltage: 1.8V ~ 3.3V (typical)

Chapter 3 Block Diagram

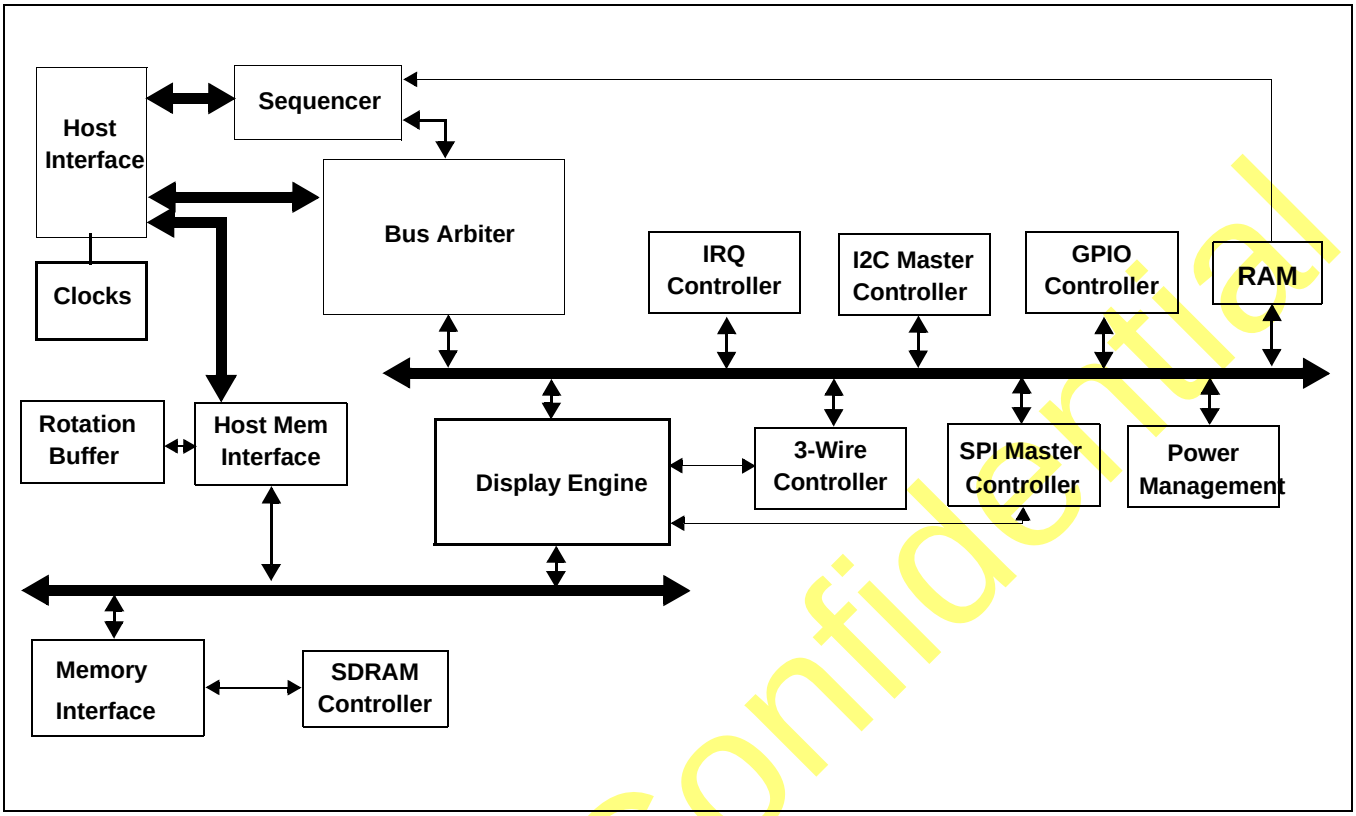


Figure 3-1: S1D13521 Block Diagram

3.1 Typical System Implementation

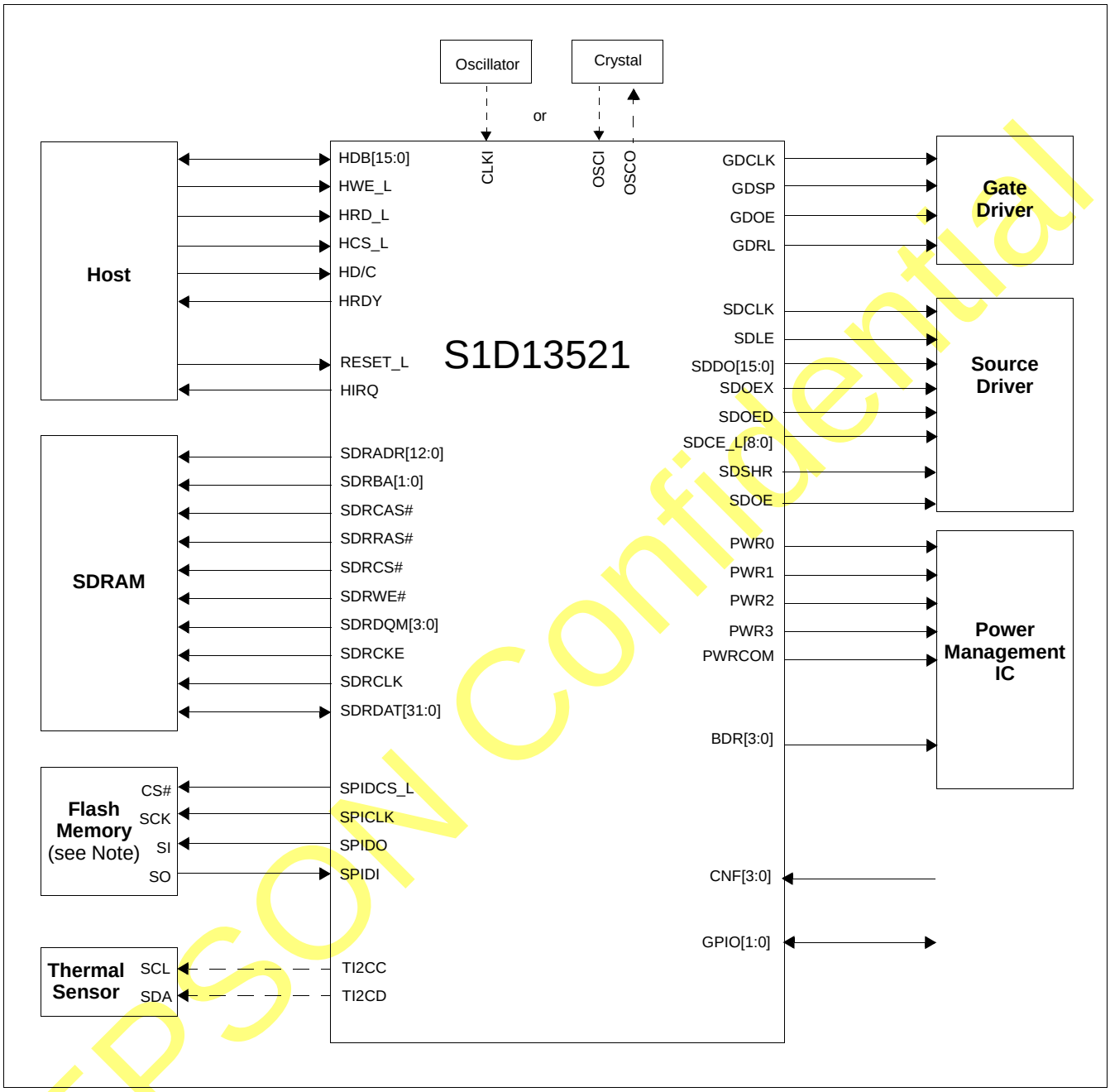


Figure 3-2: S1D13521 Typical System Implementation

Note

The Flash Memory must support the Fast Read command. For detailed Flash Memory requirements, see 17.3, “Serial Flash Memory” on page 136.

Chapter 4 Pins

4.1 Pinout Diagram

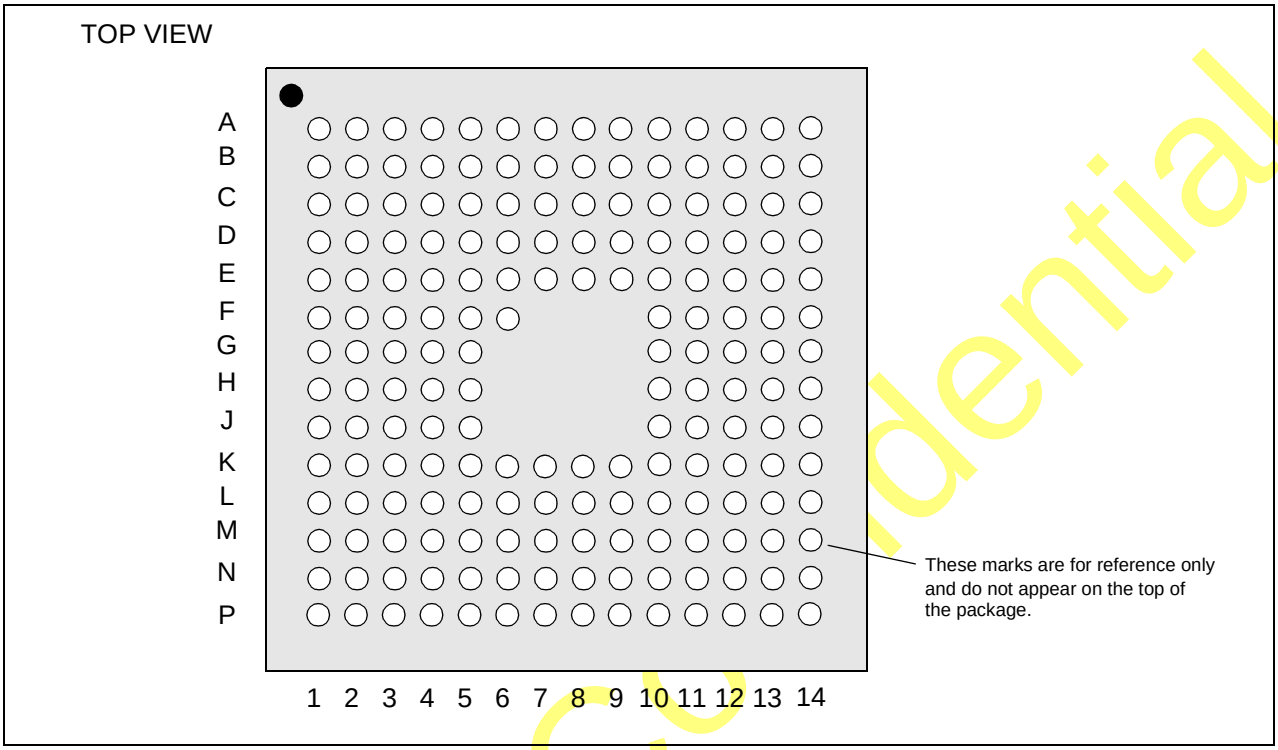


Figure 4-1: S1D13521 PFBGA8UX 181-pin Pin Mapping (Top View)

Table 4-1: S1D13521 PFBGA8UX 181-pin Pinout (Top View)

	1	2	3	4	5	6	7	8	9	10	11	12	13	14	
A	VSS	TI2CD	SPICLK	GDCLK	GDRL	SDDO14	SDDO10	PIOVDD	SDDO2	SDCE_L2	SDCE_L5	SDCE_L8	SDSHR	VSS	A
B	PWR3	PPIOVDD	TI2CC	GDSP	GDOE	SDDO13	SDDO9	SDDO5	SDDO1	SDCE_L3	SDCE_L6	SDOEX	SDOE	SDCLK	B
C	PWIOVDD	PWR1	PWR2	SPIDCS_L	SDDO15	SDDO12	SDDO8	SDDO4	SDDO0	VSS	SDCE_L7	SDOED	SDLE	SDRIOVDD	C
D	PWRCOM	BDR3	PWR0	VSS	SPIDO	SDDO11	SDDO7	SDDO3	SDCE_L0	SDCE_L4	SDRDAT26	SDRDAT24	SDRDAT21	SDRDAT23	D
E	OSCI	OSCVDD	BDR1	BDR2	SPIDI	COREVDD	SDDO6	VSS	SDCE_L1	PIOVDD	SDRDAT28	SDRDAT27	SDRDAT19	SDRDAT20	E
F	OSCO	OSCVSS	VSS	COREVDD	BDR0	VSS				VSS	SDRDAT25	SDRDAT29	SDRDAT22	VSS	F
G	VCP	PLLVSS	PLLVDD	HDB15	HDB14					COREVDD	SDRDAT30	SDRDAT31	SDRDAT18	SDRDAT17	G
H	CLKI	VSS	HIRQ	HDB13	HIOVDD					SDRIOVDD	SDRADR12	SDRDQM3	SDRDQM2	SDRDAT16	H
J	VSS	RESET_L	VSS	HRD_L	COREVDD					COREVDD	VSS	SDRADR3	SDRADR1	SDRADR2	J
K	HWE_L	CNF2	HDB12	HDB11	CNF0	HIOVDD	VSS	SDRIOVDD	COREVDD	VSS	SDRADR9	SDRADR4	SDRADR10	SDRADR0	K
L	HD/C	HDB10	HDB9	HDB8	HRDY	HCS_L	SDRDAT13	SDRDAT14	VSS	SDRWE#	SDRDQM1	SDRADR5	SDRBA1	SDRADR11	L
M	CNF1	SCANEN	GPIO1	HDB5	HDB2	SDRDAT15	SDRDAT11	SDRDAT12	SDRDAT10	SDRCAS#	SDRCS#	SDRADR6	SDRADR7	SDRRAS#	M
N	TESTEN	HDB7	HDB6	HDB4	HDB1	SDRDAT0	SDRDAT4	SDRDAT3	SDRDAT9	SDRDAT8	SDRBA0	SDRCKE	SDRIOVDD	SDRADR8	N
P	VSS	CNF3	GPIO0	HDB3	HDB0	SDRDAT2	SDRDAT1	SDRDAT6	SDRDAT5	SDRDAT7	SDRDQM0	VSS	SDRCLK	VSS	P
	1	2	3	4	5	6	7	8	9	10	11	12	13	14	

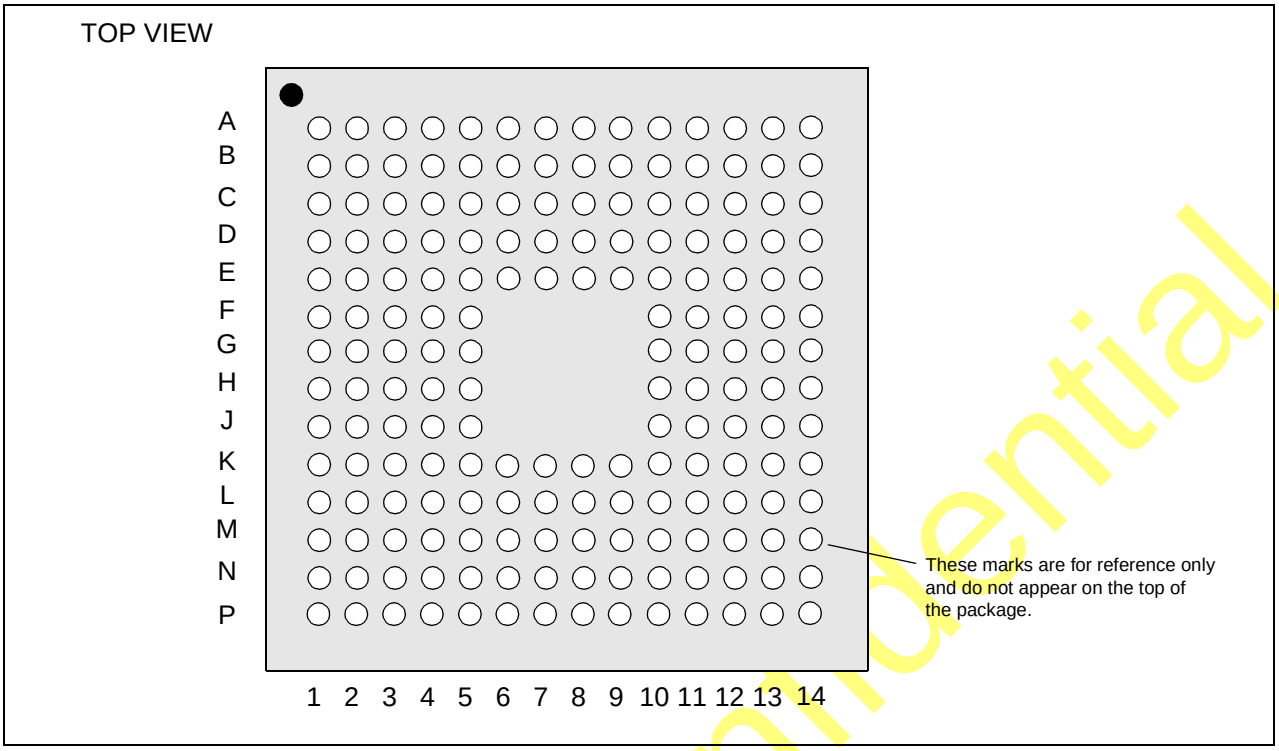


Figure 4-2: S1D13521 PFBGA12UX 180-pin Pin Mapping (Top View)

Table 4-2: S1D13521 PFBGA12UX 180-pin Pinout (Top View)

	1	2	3	4	5	6	7	8	9	10	11	12	13	14	
A	VSS	TI2CD	SPICLK	GDCLK	GDRL	SDDO14	SDDO10	PIOVDD	SDDO2	SDCE_L2	SDCE_L5	SDCE_L8	SDSHR	VSS	A
B	PWR3	PPIOVDD	TI2CC	GDSP	GDOE	SDDO13	SDDO9	SDDO5	SDDO1	SDCE_L3	SDCE_L6	SDOEX	SDOE	SDCLK	B
C	PWIOVDD	PWR1	PWR2	SPIDCS_L	SDDO15	SDDO12	SDDO8	SDDO4	SDDO0	VSS	SDCE_L7	SDOED	SDLE	SDRIOVDD	C
D	PWRCOM	BDR3	PWR0	VSS	SPIDO	SDDO11	SDDO7	SDDO3	SDCE_L0	SDCE_L4	SDRDAT26	SDRDAT24	SDRDAT21	SDRDAT23	D
E	OSCI	OSCVDD	BDR1	BDR2	SPIDI	COREVDD	SDDO6	VSS	SDCE_L1	PIOVDD	SDRDAT28	SDRDAT27	SDRDAT19	SDRDAT20	E
F	OSCO	OSCVSS	VSS	COREVDD	BDR0					VSS	SDRDAT25	SDRDAT29	SDRDAT22	VSS	F
G	VCP	PLLVSS	PLLVDD	HDB15	HDB14					COREVDD	SDRDAT30	SDRDAT31	SDRDAT18	SDRDAT17	G
H	CLKI	VSS	HIRQ	HDB13	HIOVDD					SDRIOVDD	SDRADR12	SDRDQM3	SDRDQM2	SDRDAT16	H
J	VSS	RESET_L	VSS	HRD_L	COREVDD					COREVDD	VSS	SDRADR3	SDRADR1	SDRADR2	J
K	HWE_L	CNF2	HDB12	HDB11	CNF0	HIOVDD	VSS	SDRIOVDD	COREVDD	VSS	SDRADR9	SDRADR4	SDRADR10	SDRADR0	K
L	HD/C	HDB10	HDB9	HDB8	HRDY	HCS_L	SDRDAT13	SDRDAT14	VSS	SDRWE#	SDRDQM1	SDRADR5	SDRBA1	SDRADR11	L
M	CNF1	SCANEN	GPIO1	HDB5	HDB2	SDRDAT15	SDRDAT11	SDRDAT12	SDRDAT10	SDRCAS#	SDRCS#	SDRADR6	SDRADR7	SDRRAS#	M
N	TESTEN	HDB7	HDB6	HDB4	HDB1	SDRDAT0	SDRDAT4	SDRDAT3	SDRDAT9	SDRDAT8	SDRBA0	SDRCKE	SDRIOVDD	SDRADR8	N
P	VSS	CNF3	GPIO0	HDB3	HDB0	SDRDAT2	SDRDAT1	SDRDAT6	SDRDAT5	SDRDAT7	SDRDQM0	VSS	SDRCLK	VSS	P
	1	2	3	4	5	6	7	8	9	10	11	12	13	14	

4.2 Pin Descriptions

Key:

Pin Types

I	=	Input
O	=	Output
IO	=	Bi-Directional (Input/Output)
P	=	Power pin

RESET# States

H	=	High level output
L	=	Low level output
Z	=	High Impedance (Hi-Z)
1	=	Pull-up resistor on input
0	=	Pull-down resistor on input
#	=	Active low level

Table 4-3: Cell Descriptions

Item	Description
IC	High voltage LVCMOS input buffer
ICS	High voltage LVCMOS Schmitt input buffer
ICD2	High voltage LVCMOS input buffer with pull-down (100kΩ@3.3V)
O	High voltage low noise output buffer (4mA@3.3V)
OH	High voltage high speed output buffer (4mA@3.3V)
BC	High voltage LVCMOS low noise bi-directional buffer (4mA@3.3V)
BCS	High voltage LVCMOS schmitt low noise bi-directional buffer (4mA@3.3V)
BCD2	High voltage LVCMOS low noise bi-directional buffer (4mA@3.3V) with pull-down (100kΩ@3.3V)
BCH	High voltage LVCMOS high speed bi-directional buffer (4mA@3.3V)
ILTR	Low voltage transparent input buffer
OLTR	Low voltage transparent output buffer
ILTSD	Low voltage test mode control input buffer with pull-down

Note

Unless otherwise specified, unused pins must be connected to VSS through a 100Ω resistor.

4.2.1 Shared Host Interface

Table 4-4: Shared Host Interface Pin Descriptions

Pin Name	Type	Pin #	Cell	Power	RESET_L State	Description
RESET_L	I	J2	ICS	HIOVDD	—	This active low input sets all internal registers to their default states and forces all signals to their inactive states. When unused, this pin should be connected to HIOVDD. For RESET_L timing details, see 6.3, “RESET_L Timing” on page 33.
HIRQ	O	H3	O	HIOVDD	L	This output pin is the Host IRQ.

4.2.2 Host Interface

Table 4-5: Host Interface Pin Descriptions

Pin Name	Type	Pin #	Cell	Power	RESET_L State	Description
HDB[15:0]	IO	G4, G5, H4, K3, K4, L2, L3, L4, N2, N3, M4, N4, P4, M5, N5, P5	BC	HIOVDD	Z	These pins are the shared command/parameter lines 15-0.
HWE_L	I	K1	ICS	HIOVDD	—	This input pin is the Write Enable signal.
HRD_L	I	J4	ICS	HIOVDD	—	This input pin is the Read Enable signal.
HCS_L	I	L6	IC	HIOVDD	—	This input pin is the Chip Select signal.
HD/C	I	L1	IC	HIOVDD	—	This input pin selects between Command (Low) and Parameter (High).
HRDY	IO	L5	BC	HIOVDD	H (see Note)	This active high pin is the Host interface Ready (or WAIT) signal.

Note

The RESET_L state of the HRDY pin is Low while the command sequencer loads the instruction code from the Serial Flash Memory.

4.2.3 SDRAM Interface

Table 4-6: SDRAM Interface Pin Descriptions

Pin Name	Type	Pin #	Cell	Power	RESET_L State	Description
SDRADR[12:0]	O	H11, L14, K13, K11, N14, M13, M12, L12 K12, J12, J14, J13, K14	OH	SDRIOVDD	L	These output pins are the SDRAM Address pins.
SDRBA[1:0]	O	L13, N11	OH	SDRIOVDD	L	These output pins are the SDRAM Bank Address pins.
SDRCAS#	O	M10	OH	SDRIOVDD	H	This output pin is the SDRAM CAS# pin.
SDRRAS#	O	M14	OH	SDRIOVDD	H	This output pin is the SDRAM RAS# pin.
SDRCS#	O	M11	OH	SDRIOVDD	L	This output pin is the SDRAM CS# pin.
SDRWE#	O	L10	OH	SDRIOVDD	H	This output pin is the SDRAM WE# pin.
SDRDQM[3:0]	O	H12, H13, L11, P11	OH	SDRIOVDD	H	These output pins are the SDRAM DQM pins.
SDRCKE	O	N12	OH	SDRIOVDD	H	This output pin is the SDRAM CKE pin.
SDRCLK	O	P13	OH	SDRIOVDD	H	This output pin is the SDRAM CLK pin.
SDRDAT[31:0]	IO	G12, G11, F12, E11, E12, D11, F11, D12, D14, F13, D13, E14, E13, G13, G14, H14, M6, L8, L7, M8, M7, M9, N9, N10, P10, P8, P9, N7, N8, P6, P7, N6	BCH	SDRIOVDD	L	These input/output pins are the SDRAM DATA pins.

4.2.4 SPI Master Interface for Serial Flash

Table 4-7: SPI Master Interface Pin Descriptions

Pin Name	Type	Pin #	Cell	Power	RESET_L State	Description
SPIDCS_L	O	C4	O	PPIOVDD	H	This output pin is the Slave Chip Select for the SPI interface.
SPICLK	O	A3	O	PPIOVDD	L	This output pin is the Slave Clock for the SPI interface.
SPIDO	O	D5	O	PPIOVDD	L	This pin is the data output for the SPI interface.
SPIDI	I	E5	IC	PPIOVDD	—	This pin is the data input for the SPI interface.

4.2.5 I2C Master Interface for Thermal Sensor

Table 4-8: I2C Master Interface Pin Descriptions

Pin Name	Type	Pin #	Cell	Power	RESET_L State	Description
TI2CC	IO	B3	BCS	PPIOVDD	Z	This input/output pin is the I2C Master Serial Clock. If this pin is not used, it must be connected to PPIOVDD.
TI2CD	IO	A2	BCS	PPIOVDD	Z	This input/output pin is the I2C Master Data. If this pin is not used, it must be connected to PPIOVDD.

4.2.6 Gate Driver Interface

Table 4-9: Gate Driver Interface Pin Descriptions

Pin Name	Type	Pin #	Cell	Power	RESET_L State	Description
GDCLK	O	A4	O	PIOVDD	L	This output pin is the clock for the Gate Driver.
GDSP	O	B4	O	PIOVDD	H	This output pin is the Gate Driver Start Pulse.
GDOE	O	B5	O	PIOVDD	L	This output pin is the output enable for the Gate Driver.
GDRL	O	A5	O	PIOVDD	L	This output pin is the Gate Driver Right or Left.

4.2.7 Source Driver Interface

Table 4-10: Source Driver Interface Pin Descriptions

Pin Name	Type	Pin #	Cell	Power	RESET_L State	Description
SDCLK	O	B14	O	PIOVDD	L	This output pin is the clock for the Source Driver.
SDLE	O	C13	O	PIOVDD	L	This output pin is the latch enable for the Source Driver.
SDDO[15:0]	O	C5, A6, B6, C6, D6, A7, B7, C7, D7, E7, B8, C8, D8, A9, B9, C9	O	PIOVDD	L	These are the data output pins for the Source Driver.
SDOED	O	C12	O	PIOVDD	L	This output is the SDOED pin used for Double Data Rate Source Driver output.
SDOEX	O	B12	O	PIOVDD	L	This output is the SDOEX pin used for Double Data Rate Source Driver output.
SDCE_L[8:0]	O	A12, C11, B11, A11, D10, B10, A10, E9, D9	O	PIOVDD	H	These output pins are the Source Driver Chip Enables 8-0. For details on the configurability of these pins, refer to A.3.14, “Display Engine: Driver Configurations” on page 208 (see REG[030Ch]) and 6.5.2, “Interpreted Source Driver Timings” on page 39.
SDSHR	O	A13	O	PIOVDD	L	This output pin is the Source Driver Shift Right Enable.
SDOE	O	B13	O	PIOVDD	L	This output pin is the output enable for the Source Driver.

4.2.8 Power Switches Control Interface

The power control interface signals have dual function pins.
1. Power sequence output (default power-on function)
2. 3-wire Active Matrix Power Management ICs

Table 4-11: Power Switches Control Interface Pin Descriptions

Pin Name	Type	Pin #	Cell	Power	RESET_L State	Description
PWR0/ DAPWRALL	IO	D3	BC	PWIOVDD	L	These input/output pins have multiple functions. • Power Control Signal 0 (PWR0). For timing details, see 6.6.1, “Power Pin Transition Sequence for PWR[3:0]” on page 48. • 3-wire Power All Pin output (DAPWRALL)
PWR1/DACLK	IO	C2	BC	PWIOVDD	L	These input/output pins have multiple functions. • Power Control Signal 1 (PWR1). For timing details, see 6.6.1, “Power Pin Transition Sequence for PWR[3:0]” on page 48. • 3-wire Serial Clock (DACLK)
PWR2/DADIO	IO	C3	BC	PWIOVDD	L	These input/output pins have multiple functions. • Power Control Signal 2 (PWR2). For timing details, see 6.6.1, “Power Pin Transition Sequence for PWR[3:0]” on page 48. • 3-wire data tri-state input/output (DADIO)
PWR3/ DACEB	IO	B1	BC	PWIOVDD	L	These input/output pins have multiple functions. • Power Control Signal 3 (PWR3). For timing details, see 6.6.1, “Power Pin Transition Sequence for PWR[3:0]” on page 48. • 3-wire active low enable (DACEB)
PWRCOM	O	D1	O	PWIOVDD	L	Display Common Power Signals. For timing details, see 6.6.2, “Power Pin Transition Sequence for PWRCOM” on page 49.

4.2.9 Display Border Power Interface

Table 4-12: Display Border Power Interface Pin Descriptions

Pin Name	Type	Pin #	Cell	Power	RESET_L State	Description
BDR[3:0]	O	D2, E4, E3, F5	O	PWIOVDD	L	These output pins are the Display Border Power Signals.

4.2.10 Miscellaneous

Table 4-13: Miscellaneous Pin Descriptions

Pin Name	Type	Pin #	Cell	Power	RESET_L State	Description
CLKI	I	H1	ICS	HIOVDD	—	This pin is the clock input. For details on the clock structure, see Chapter 7, “Clocks” on page 50. If unused, this pin must be connected to VSS.
OSCI	I	E1	ILTR	OSCVDD	—	This pin is the input for the 2-terminal crystal interface. When the internal oscillator is not used, this pin must be connected to OSCVDD. For details on the clock structure, see Chapter 7, “Clocks” on page 50.
OSCO	O	F1	OLTR	OSCVDD	H	This pin is the output for the 2-terminal crystal interface. When the internal oscillator is not used, this pin must be left unconnected. For details on the clock structure, see Chapter 7, “Clocks” on page 50.
CNF[3:0]	I	P2, K2, M1, K5	IC	HIOVDD	—	These input pins are used for configuring the S1D13521 and must be connected to either HIOVDD or VSS. For a summary of configuration options, see 4.3, “Configuration Pins” on page 24.
GPIO[1:0]	IO	M3, P3	BCD2	HIOVDD	Z	These are the General Purpose Input/Output pins.
TESTEN	I	N1	ILTSD	HIOVDD	—	This input pin is the Test Enable pin and is used for production test only. This pin should be left unconnected for normal operation.
SCANEN	I	M2	ICD2	HIOVDD	—	This input pin is the Scan Enable pin and is used for production test only. This pin should be left unconnected for normal operation.
VCP	O	G1	OLTR	PLLVDD	—	This output pin is for production test only and must be left unconnected for normal operation.

4.2.11 Power and Ground

Table 4-14: Power And Ground Pin Descriptions

Pin Name	Type	Pin#	Cell	Power	RESET_L State	Description
HIOVDD	P	H5, K6	P	1.65-3.6V	—	IO power supply for the Host interface
SDRIOVDD	P	C14, H10, K8, N13	P	1.8/3.3V	—	IO power supply for the SDRAM interface
PPIOVDD	P	B2	P	1.65-3.6V	—	IO power supply for the SPI and I2C interface
PWIOVDD	P	C1	P	1.65-3.6V	—	IO power supply for Power Switch & Display Border control
PIOVDD	P	A8, E10	P	1.65-3.6V	—	IO power supply for Source and Gate Driver
COREVDD	P	E6, F4, G10, J5, J10, K9	P	1.8V	—	Core power supply
VSS (see Note)	P	A1, A14, C10, D4, E8, F3, F6, F10, F14, H2, J1, J3, J11, K7, K10, L9, P1, P12, P14	P	0	—	GND for HIOVDD, SDRIOVDD, PPIOVDD, PWIOVDD, PIOVDD, and COREVDD
PLLVDD	P	G3	P	1.8V	—	PLL power supply
PLLVSS	P	G2	P	0	—	GND for PLLVDD
OSCVDD	P	E2	P	1.8V	—	OSC power supply
OSCVSS	P	F2	P	0	—	GND for OSCVDD

Note
For the PFBGA12UX 180-pin package, there is no F6 pin.

4.3 Configuration Pins

The S1D13521 has four configuration pins, CNF[3:0], which must be connected to HIOVDD or VSS according to the following table.

Table 4-15: Configuration Pin Summary

CNF[3:0]	1 (connected to HIOVDD)	0 (connected to VSS)
CNF3	HRDY only driven when HCS_L is asserted	HRDY is always driven
CNF2	OSCI/OSCO is the source for the Input Clock. (see Note)	CLKI is the source for the Input Clock.
CNF1	Reserved. This pin must be connected to HIOVDD.	
CNF0	Reserved. This pin must be connected to VSS.	

Note
When using the internal oscillator (CNF2=1), there are timing requirements that must be observed or the Command Interface hardware will not be able to perform a normal boot-up initialization sequence which will result in a system failure for the S1D13521. For details on these timing requirements, refer to Chapter 18, “OSC Clock Timing Requirements” on page 145.

4.4 Pin Mapping

4.4.1 Source Driver Interface

The Source Driver output width is dependent on the Pixel Output Count Select bit (see REG[030Ch] bit 11).

Table 4-16: Source Driver Interface Bitwidth Select

Pin Name	Pixel Output Count Select = 0 (4 pixels per SDCLK)		Pixel Output Count Select = 1 (8 pixels per SDCLK)	
	2-bit Voltage Level Control	4-bit Voltage Level Control	2-bit Voltage Level Control	4-bit Voltage Level Control
SDCLK	SDCLK	SDCLK	SDCLK	No Supported Mode
SDLE	SDLE	SDLE	SDLE	
SDDO[1:0]	Pixel 0[1:0]	Pixel 0[1:0]	Pixel 0[1:0]	
SDDO[3:2]	Pixel 1[1:0]	Pixel 0[2:3]	Pixel 1[1:0]	
SDDO[5:4]	Pixel 2[1:0]	Pixel 1[1:0]	Pixel 2[1:0]	
SDDO[7:6]	Pixel 3[1:0]	Pixel 1[2:3]	Pixel 3[1:0]	
SDDO[9:8]	driven 0	Pixel 2[1:0]	Pixel 4[1:0]	
SDDO[11:10]	driven 0	Pixel 2[2:3]	Pixel 5[1:0]	
SDDO[13:12]	driven 0	Pixel 3[1:0]	Pixel 6[1:0]	
SDDO[15:14]	driven 0	Pixel 3[2:3]	Pixel 7[1:0]	
SDOED	driven 0	driven 0	driven 0 for non-DDR SDOED for DDR	
SDOEX	driven 0	driven 0	driven 0 for non-DDR SDOEX for DDR	
SDCE_L[8:0]	SDCE_L[8:0]	SDCE_L[8:0]	SDCE_L[8:0]	
SDSHR	SDSHR	SDSHR	SDSHR	
SDOE	SDOE	SDOE	SDOE	

4.4.2 Border Pin Interface

Table 4-17: Border Pin Interface Bitwidth Select

Pin Name	2-bit Voltage Level Control	4-bit Voltage Level Control
BDR[1:0]	Border Value[1:0]	Border Value[1:0]
BDR[3:2]	Driven 0	Border Value[2:3]

Chapter 5 D.C. Characteristics

5.1 Absolute Maximum Ratings

Table 5-1: Absolute Maximum Ratings

Symbol	Parameter	Rating	Units
Core V_{DD}	Core Supply Voltage	V_{SS} - 0.3 ~ 2.5	V
PLL V_{DD}	PLL Supply Voltage	V_{SS} - 0.3 ~ 2.5	V
OSC V_{DD}	OSC Supply Voltage	V_{SS} - 0.3 ~ 2.5	V
HIO V_{DD}	Host IO Supply Voltage	V_{SS} - 0.3 ~ 4.0	V
PIO V_{DD}	Gate/Source IO Supply Voltage	V_{SS} - 0.3 ~ 4.0	V
SDRIO V_{DD}	SDRAM IO Supply Voltage	V_{SS} - 0.3 ~ 4.0	V
PPIO V_{DD}	SPI and I2C IO Supply Voltage	V_{SS} - 0.3 ~ 4.0	V
PWIO V_{DD}	Power Switch Control IO Supply Voltage	V_{SS} - 0.3 ~ 4.0	V
V_{IN}	Input Signal Voltage	V_{SS} - 0.3 ~ *IO V_{DD} + 0.5	V
V_{OUT}	Output Signal Voltage	V_{SS} - 0.3 ~ *IO V_{DD} + 0.5	V
I_{OUT}	Output Signal Current	±10	mA
T_{STG}	Storage Temperature	-65 ~ 150	°C

Note
V_{SS} = 0 V
Core V_{DD}, PLL V_{DD}, OSC V_{DD} ≤ *IOV_{DD}

5.2 Recommended Operating Conditions

Table 5-2: Recommended Operating Conditions

Symbol	Parameter	Condition	Min	Typ	Max	Units
Core V_{DD}	Core Supply Voltage	V_{SS} = 0 V	1.65	1.80	1.95	V
PLL V_{DD}	PLL Supply Voltage	V_{SS} = 0 V	1.65	1.80	1.95	V
OSC V_{DD}	OSC Supply Voltage	V_{SS} = 0 V	1.65	1.80	1.95	V
HIO V_{DD}	Host IO Supply Voltage	V_{SS} = 0 V	1.65	—	3.60	V
PIO V_{DD}	Gate/Source IO Supply Voltage	V_{SS} = 0 V	1.65	—	3.60	V
SDRIO V_{DD}	SDRAM IO Supply Voltage	V_{SS} = 0 V	1.65	1.80	1.95	V
		V_{SS} = 0 V	2.70	3.30	3.60	V
PPIO V_{DD}	SPI and I2C IO Supply Voltage	V_{SS} = 0 V	1.65	—	3.60	V
PWIO V_{DD}	Power Switch Control IO Supply Voltage	V_{SS} = 0 V	1.65	—	3.60	V
V_{IN}	Input Voltage	—	V_{SS}	—	*IO V_{DD}	V
T_{OPR}	Operating Temperature	—	-40	25	85	°C

5.3 Electrical Characteristics

Table 5-3: Electrical Characteristics for IO V_{DD} = 1.8V ± 0.15V

Symbol	Parameter	Condition	Min	Typ	Max	Units
I_{DDS}	Quiescent Current	Quiescent Conditions	—	1.4	—	µA
I_{IZ}	Input Leakage Current	—	-5	—	5	µA
I_{OZ}	Output Leakage Current	—	-5	—	5	µA
I_{OH}	High Level Output Current	IOV_{DD} = min V_{OH} = IO V_{DD} - 0.4 V	-2	—	—	mA
I_{OL}	Low Level Output Current	IOV_{DD} = min V_{OL} = 0.4 V	2	—	—	mA
V_{IH}	High Level Input Voltage	LVCMOS Level IO V_{DD} = max	1.27	—	IO V_{DD} + 0.3	V
V_{IL}	Low Level Input Voltage	LVCMOS Level IO V_{DD} = min	-0.3	—	0.57	V
V_{T+}	Positive Trigger Voltage	LVCMOS Schmitt	0.58	—	1.46	V
V_{T-}	Negative Trigger Voltage	LVCMOS Schmitt	0.42	—	1.26	V
V_H	Hysteresis Voltage	LVCMOS Schmitt	0.17	—	—	V
R_{PD}	Pull-Down Resistance	V_{IN} = IO V_{DD}	96	240	600	kΩ
C_I	Input Pin Capacitance	f = 1MHz, IO V_{DD} = 0V	—	—	6	pF
C_O	Output Pin Capacitance	f = 1MHz, IO V_{DD} = 0V	—	—	6	pF
C_{IO}	Bi-Directional Pin Capacitance	f = 1MHz, IO V_{DD} = 0V	—	—	6	pF

Table 5-4: Electrical Characteristics for IO V_{DD} = 2.5V ± 0.2V

Symbol	Parameter	Condition	Min	Typ	Max	Units
I_{DDS}	Quiescent Current	Quiescent Conditions	—	1.4	—	µA
I_{IZ}	Input Leakage Current	—	-5	—	5	µA
I_{OZ}	Output Leakage Current	—	-5	—	5	µA
I_{OH}	High Level Output Current	IOV_{DD} = min V_{OH} = IO V_{DD} - 0.4 V	-3	—	—	mA
I_{OL}	Low Level Output Current	IOV_{DD} = min V_{OL} = 0.4 V	3	—	—	mA
V_{IH}	High Level Input Voltage	LVCMOS Level IO V_{DD} = max	1.7	—	IO V_{DD} + 0.3	V
V_{IL}	Low Level Input Voltage	LVCMOS Level IO V_{DD} = min	-0.3	—	0.7	V
V_{T+}	Positive Trigger Voltage	LVCMOS Schmitt	0.92	—	1.89	V
V_{T-}	Negative Trigger Voltage	LVCMOS Schmitt	0.58	—	1.48	V
V_H	Hysteresis Voltage	LVCMOS Schmitt	0.23	—	—	V
R_{PD}	Pull-Down Resistance	V_{IN} = IO V_{DD}	70	140	350	kΩ
C_I	Input Pin Capacitance	f = 1MHz, IO V_{DD} = 0V	—	—	6	pF
C_O	Output Pin Capacitance	f = 1MHz, IO V_{DD} = 0V	—	—	6	pF
C_{IO}	Bi-Directional Pin Capacitance	f = 1MHz, IO V_{DD} = 0V	—	—	6	pF

Table 5-5: Electrical Characteristics for IO V_{DD} = 3.3V ± 0.3V

Symbol	Parameter	Condition	Min	Typ	Max	Units
I_{DDS}	Quiescent Current	Quiescent Conditions	—	1.4	—	µA
I_{IZ}	Input Leakage Current	—	-5	—	5	µA
I_{OZ}	Output Leakage Current	—	-5	—	5	µA
I_{OH}	High Level Output Current	IOV_{DD} = min V_{OH} = IO V_{DD} - 0.4 V	-4	—	—	mA
I_{OL}	Low Level Output Current	IOV_{DD} = min V_{OL} = 0.4 V	4	—	—	mA
V_{IH}	High Level Input Voltage	LVCMOS Level IO V_{DD} = max	2.2	—	IO V_{DD} + 0.3	V
V_{IL}	Low Level Input Voltage	LVCMOS Level IO V_{DD} = min	-0.3	—	0.8	V
V_{T+}	Positive Trigger Voltage	LVCMOS Schmitt	1.2	—	2.52	V
V_{T-}	Negative Trigger Voltage	LVCMOS Schmitt	0.75	—	1.98	V
V_H	Hysteresis Voltage	LVCMOS Schmitt	0.3	—	—	V
R_{PD}	Pull-Down Resistance	V_{IN} = IO V_{DD}	50	100	240	kΩ
C_I	Input Pin Capacitance	f = 1MHz, IO V_{DD} = 0V	—	—	6	pF
C_O	Output Pin Capacitance	f = 1MHz, IO V_{DD} = 0V	—	—	6	pF
C_{IO}	Bi-Directional Pin Capacitance	f = 1MHz, IO V_{DD} = 0V	—	—	6	pF

Table 5-6: Electrical Characteristics for CORE V_{DD}

Symbol	Parameter	Condition	Min	Typ	Max	Units
I_{DDS}	Quiescent Current	Quiescent Conditions	—	2.2	—	µA
I_{IZ}	Input Leakage Current	—	-5	—	5	µA
I_{OZ}	Output Leakage Current	—	-5	—	5	µA

Table 5-7: Electrical Characteristics for PLL V_{DD}

Symbol	Parameter	Condition	Min	Typ	Max	Units
I_{DDS}	Quiescent Current	Quiescent Conditions	—	0.1	—	µA
I_{IZ}	Input Leakage Current	—	-5	—	5	µA
I_{OZ}	Output Leakage Current	—	-5	—	5	µA

Chapter 6 A.C. Characteristics

Conditions:

IOVDD = 1.65V to 3.60V
TA = -40°C to 85°C
Trise and Tfall for all inputs except Schmitt and CLKI must be < 50 ns (10% ~ 90%)
Trise and Tfall for all Schmitt must be < 5 ms (10% ~ 90%)
CL = 10pF (SDRCLK and SDRDAT[31:0])
CL = 15pF (All SDRAM signals except SDRCLK and SDRDAT[31:0])
CL = 30pF (HDB[15:0] and HRDY)
CL = 45pF (Gate Driver and Source Driver Interfaces)
CL = 15pF (Power Switches Control Interface)
CL = 30pF (GPIO Interface)
CL = 20pF (I2C Interface)
CL = 15pF (SPI Interface)

6.1 Clock Timing

6.1.1 Input Clocks

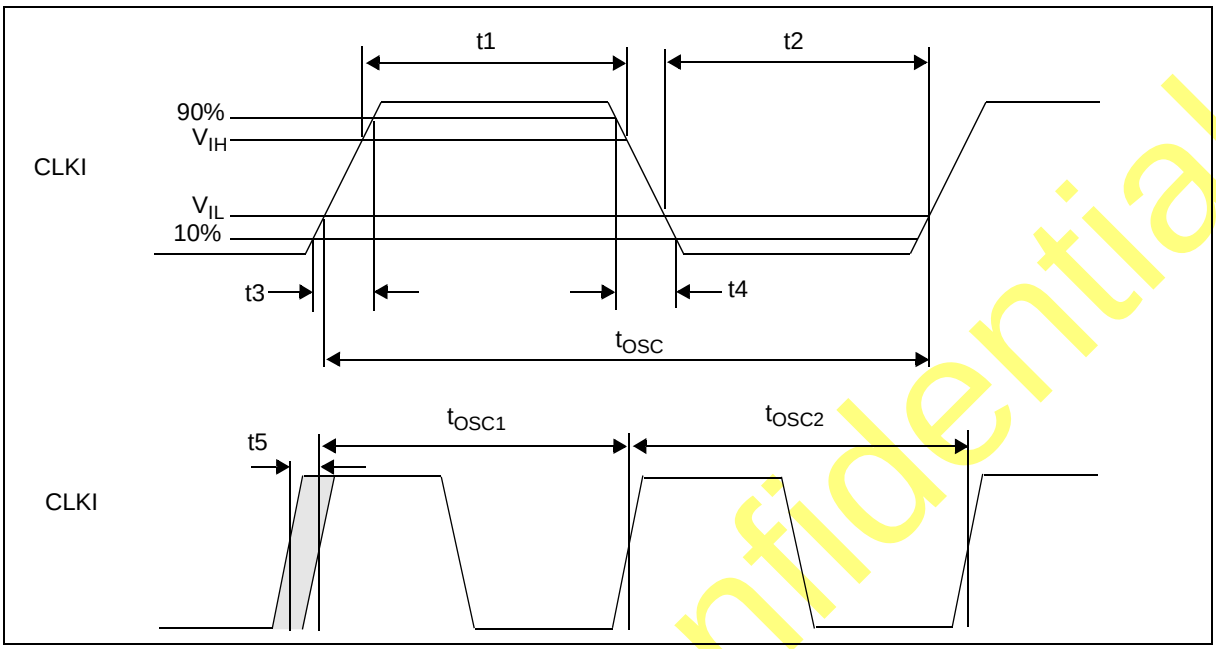


Figure 6-1 Clock Input Requirements (CLKI)

Table 6-1 Clock Input Requirements

Symbol	Parameter	Min	Typ	Max	Units
f_{OSC}	Input clock frequency of CLKI when PLL used for System Clock (see Note 1)	20	—	66.5	MHz
	Input clock frequency of CLKI when CLKI used for System Clock	0	—	133	MHz
	Input clock frequency of OSC when PLL used for System Clock (see Note 1)	24	—	27	MHz
t_{OSC}	Input clock period	—	$1/f_{OSC}$	—	µs
t1	Input clock pulse width high (see Note 2)	$0.4t_{OSC}$	—	$0.6t_{OSC}$	µs
t2	Input clock pulse width low (see Note 2)	$0.4t_{OSC}$	—	$0.6t_{OSC}$	µs
t3	Input clock rise time (10% - 90%)	—	—	500	ps
t4	Input clock fall time (90% - 10%)	—	—	500	ps
t5 (see Note 3)	Input clock cycle jitter (see Notes 4 and 5)	-150		150	ps

1. To achieve the maximum possible PLL output frequency, the input source frequency must be evenly divisible into 133 MHz. For further details on programming the PLL, see A.3.2, “Clock Configuration Registers” on page 166.
2. Input Duty cycle is not critical and can be 40/60.
3. $t5 = t_{OSC1} - t_{OSC2}$
4. The input clock cycle jitter is the difference in period between adjacent cycles.
5. The jitter characteristics must satisfy the t5 characteristics

6.1.2 PLL Clock

The PLL circuit is an analog circuit and is very sensitive to noise on the input clock waveform or the power supply. Noise on the clock or the supplied power may cause the operation of the PLL circuit to become unstable or increase the jitter.

Due to these noise constraints, it is highly recommended that the power supply traces or the power plane for the PLL be isolated from those of other power supplies. Filtering should also be used to keep the power as clean as possible. The jitter of the input clock waveform should be as small as possible.

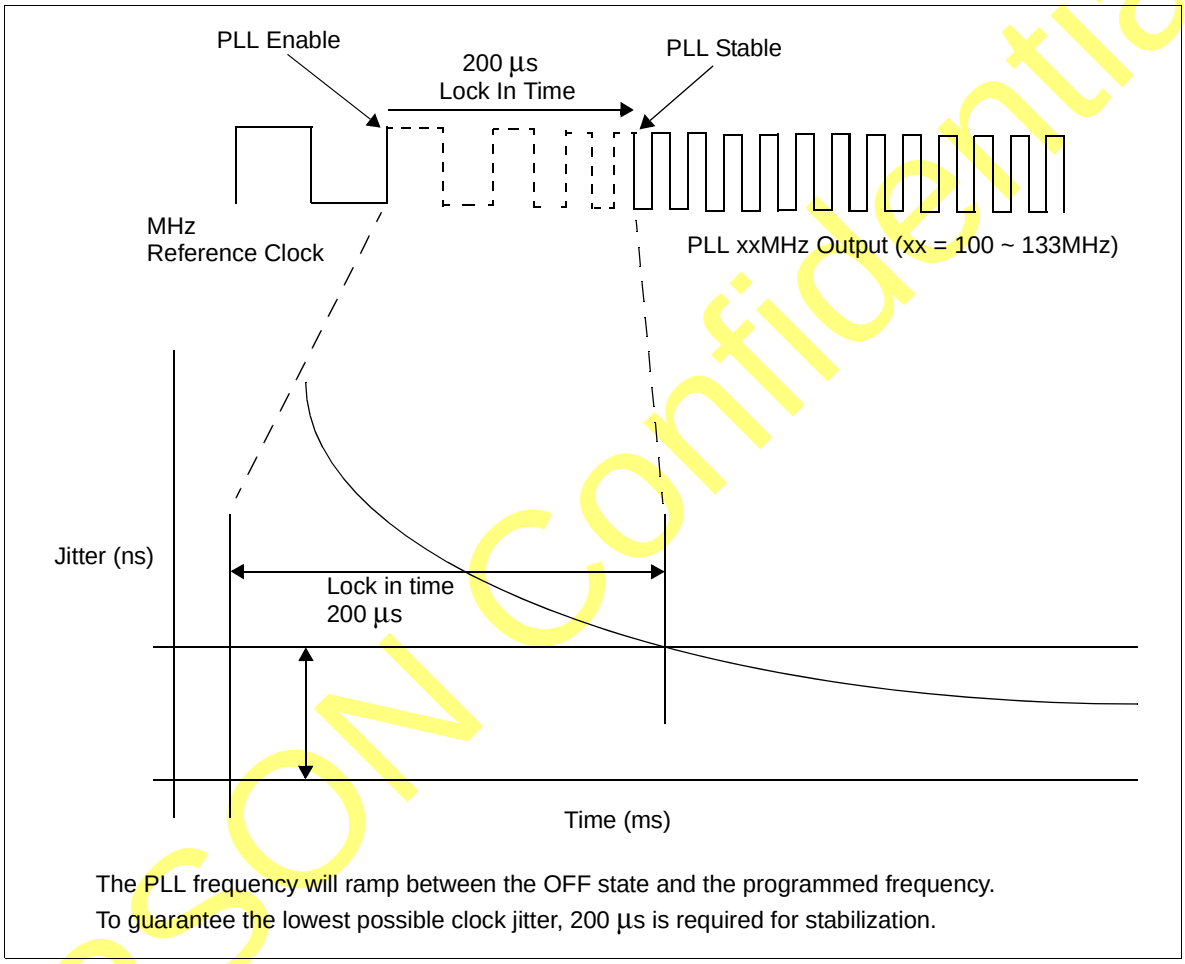


Figure 6-2: PLL Start-Up Time

Table 6-2: PLL Clock Requirements

Symbol	Parameter	Min	Max	Units
f_{PLL}	PLL output clock frequency	100	133	MHz
t_{PJref}	PLL output clock period jitter	-2	2	%
t_{PDuty}	PLL output clock duty cycle	45	55	%
t_{PStal}	PLL output stable time	—	200	µs

6.2 Power Supply Sequence

6.2.1 Power-On Sequence

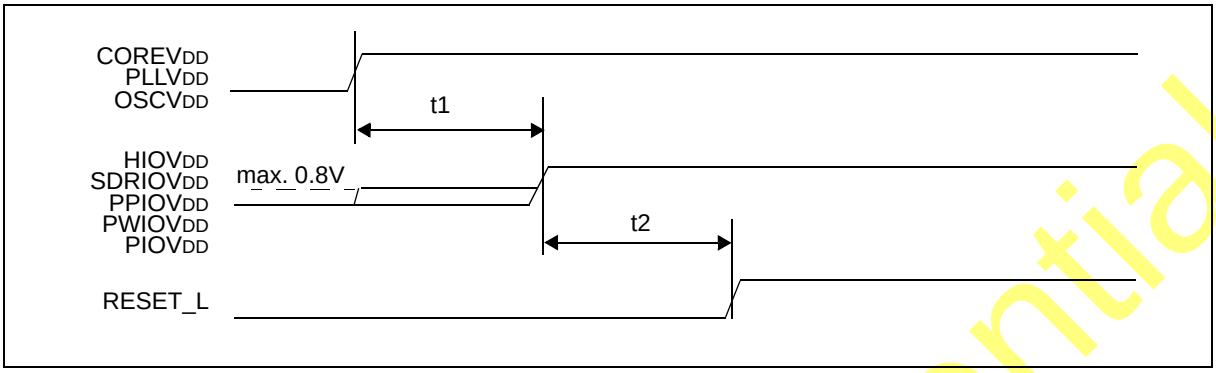


Figure 6-3: Power-On Sequence

Table 6-3: Power-On Sequence

Symbol	Parameter	Min	Max	Units
t1	HIOVDD, SDRIOVDD, PPIOVDD, PWIOVDD, PIOVDD on delay from COREVDD, PLLVDD, OSCVDD on	0	500	ms
t2	RESET_L deasserted from HIOVDD, SDRIOVDD, PPIOVDD, PWIOVDD, PIOVDD on	Note 1	—	ns

1. For RESET_L timing details, refer to 6.3, “RESET_L Timing” on page 33.

6.2.2 Power-Off Sequence

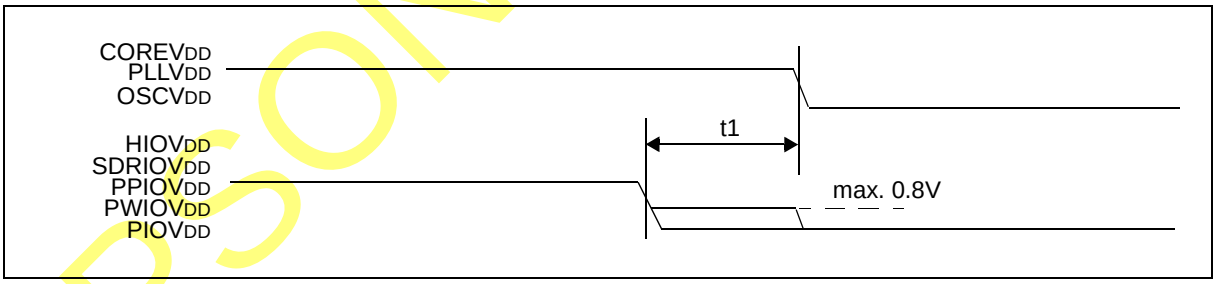


Figure 6-4: Power-Off Sequence

Table 6-4: Power-Off Sequence

Symbol	Parameter	Min	Max	Units
t1	COREVDD, PLLVDD, OSCVDD off delay from HIOVDD, SDRIOVDD, PPIOVDD, PWIOVDD, PIOVDD off	0	500	ms

6.3 RESET_L Timing

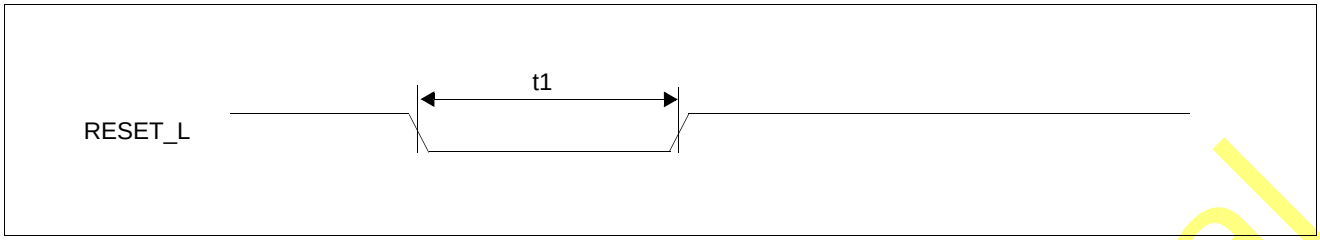


Figure 6-5 S1D13521 RESET_L Timing

Table 6-5 S1D13521 RESET_L Timing

Symbol	Parameter	Min	Max	Units
t1	Active Reset Pulse Width when using CLKI	200	—	ns
	Active Reset Pulse Width when using OSCI/OSCO	4 (Note 1)	—	ms

1 The minimum active reset pulse width when using OSCI/OSCO is based on the example external OSC circuit described in Chapter 18, “OSC Clock Timing Requirements” on page 145.

Note
For further information on RESET_L timing, see Chapter 18, “OSC Clock Timing Requirements” on page 145.

6.4 Host Interface Timing

6.4.1 16-bit Host Interface Timing (Intel 80)

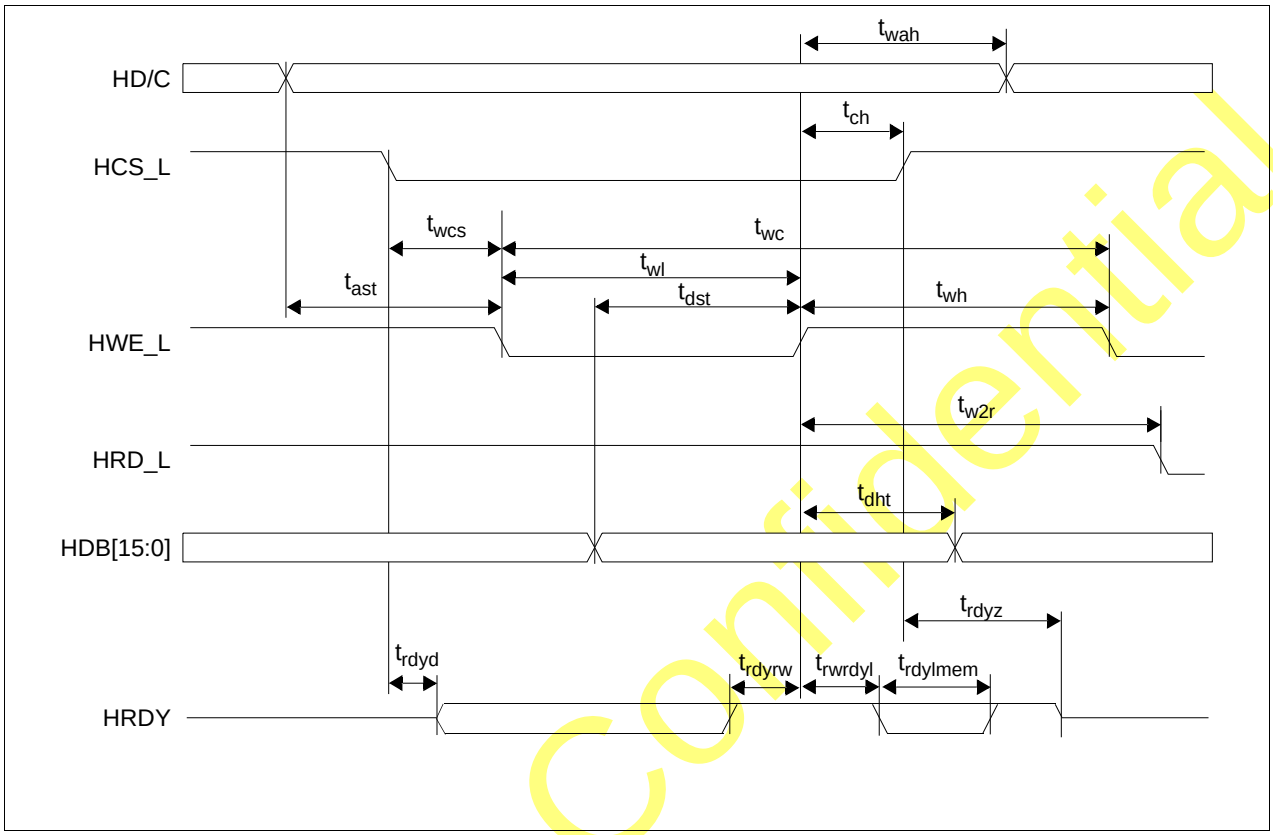


Figure 6-6: 16-bit Host Interface (Intel 80) Write Timing

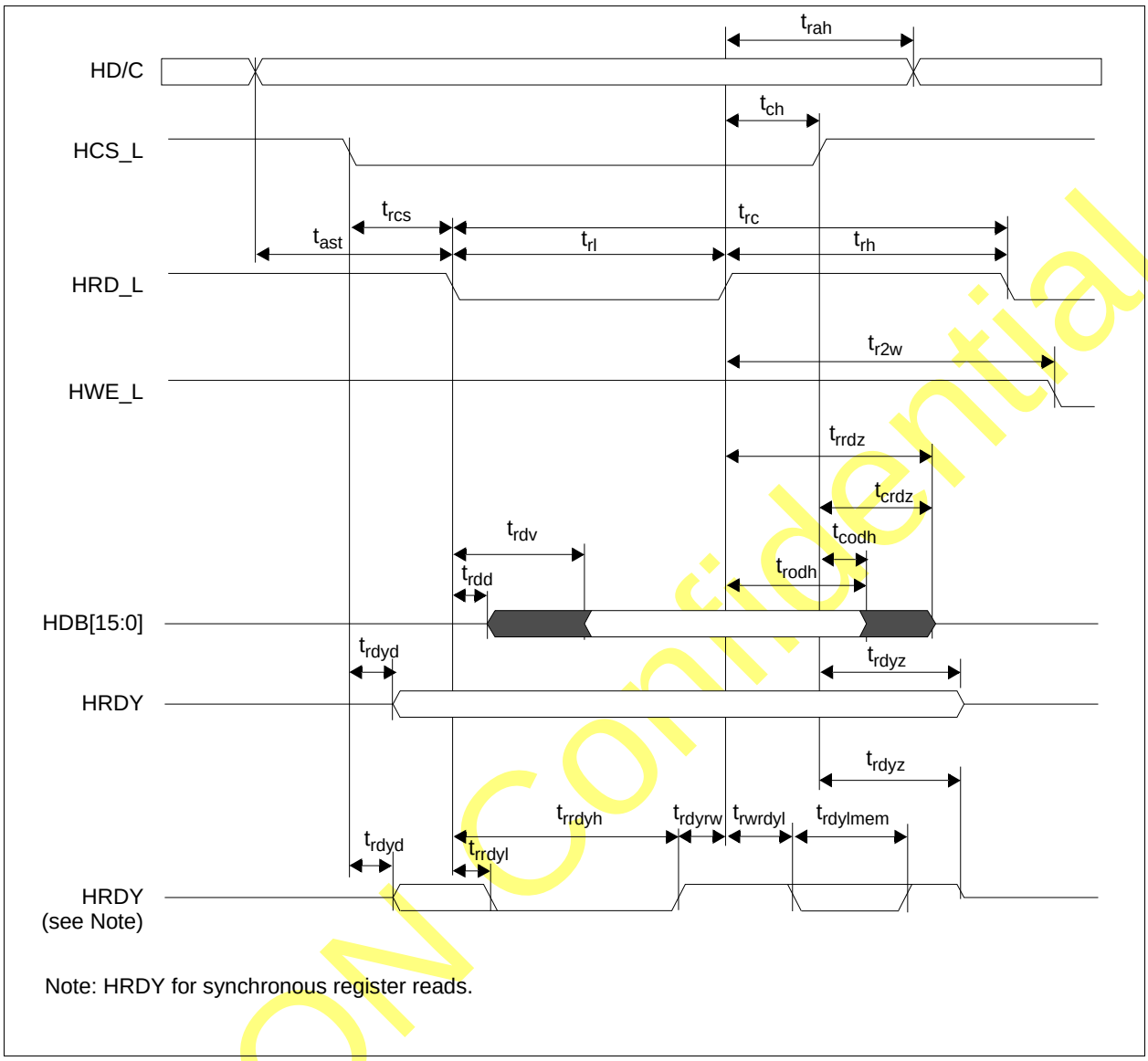


Figure 6-7: 16-bit Host Interface (Intel 80) Read Timing

Table 6-6: 16-bit Host Interface (Intel 80) A.C. Characteristics - 1.8 Volt

Signal	Symbol	Parameter	Min	Max	Unit	Description
HD/C	t_{ast}	Address setup time (read/write)	0	—	ns	
	t_{wah}	Address hold time (write)	5	—	ns	
	t_{rah}	Address hold time (read)	6	—	ns	
HCS_L	t_{wcs}	Chip Select setup time to HWR_L falling edge	1	—	ns	
	t_{rcs}	Chip Select setup time to HRD_L falling edge	1	—	ns	
	t_{ch}	Chip Select hold time (read/write)	5	—	ns	
HWE_L	t_{wl}	Pulse low duration	7	—	ns	
	t_{wh}	Pulse high duration	7	—	ns	
	t_{wc}	Write cycle for Registers	5	—	Ts (Note 1)	
		Write cycle for Memory	4	—	Ts	
	t_{w2r}	HWR_L rising edge to HRD_L falling edge	2	—	Ts	
HRD_L	t_{r2w}	HRD_L rising edge to HWR_L falling edge	0	—	ns	
	t_{rc}	Read cycle for Registers	5	—	Ts	
		Read cycle for Memory	4	—	Ts	
	t_{rl}	Pulse low duration (for Registers)	4T + 24	—	ns	
		Pulse low duration (for Memory)	3T + 23	—	ns	
	t_{rh}	Pulse high duration	4	—	ns	
HDB[15:0]	t_{dst}	Write data setup time	7	—	ns	
	t_{dht}	Write data hold time	6	—	ns	
	t_{rodh}	Read data hold time from HRD_L rising edge	2	9	ns	
	t_{rrdz}	HRD_L rising edge to HDB[15:0] Hi-Z	2	9	ns	
	t_{rdv}	HRD_L falling edge to HDB[15:0] valid for Registers	—	4T + 23	ns	CL=30pF
		HRD_L falling edge to HDB[15:0] valid for Memory (if t_{rc} not met)	—	3T + 22	ns	
	t_{rdd}	HRD_L falling edge to HDB[15:0] driven	4	—	ns	CL=30pF
HRDY	t_{rdyd}	HCS_L falling edge to HRDY driven	—	11	ns	CL=30pF
	t_{rdyz}	HCS_L rising edge to HRDY Hi-Z	—	5	ns	CL=30pF
	t_{rrdyl}	HRD_L falling edge to HRDY low	—	18	ns	CL=30pF
	t_{rrdyh}	HRD_L falling edge to HRDY high	—	4T + 24	ns	CL=30pF
	t_{rdyrw}	HRDY rising edge to HRD_L/HWE_L rising edge	T - 13	—	ns	CL=30pF
	t_{rwrdyl}	HWE_L rising edge to HRDY falling edge (for Command accesses)	—	17	ns	CL=30pF
		HRD_L/HWE_L rising edge to HRDY falling edge (for Memory accesses)	—	16	ns	CL=30pF
	$t_{rdylmem}$	HRDY low period for memory read/write	—	3	Ts	CL=30pF

1. Ts = System Clock period

6.5 Display Timings

The following figure provides an overview of the S1D13521 display frame settings. For detailed display timings, refer to 6.5.2, “Interpreted Source Driver Timings” on page 39 and 6.5.3, “Interpreted Gate Driver Timings” on page 46.

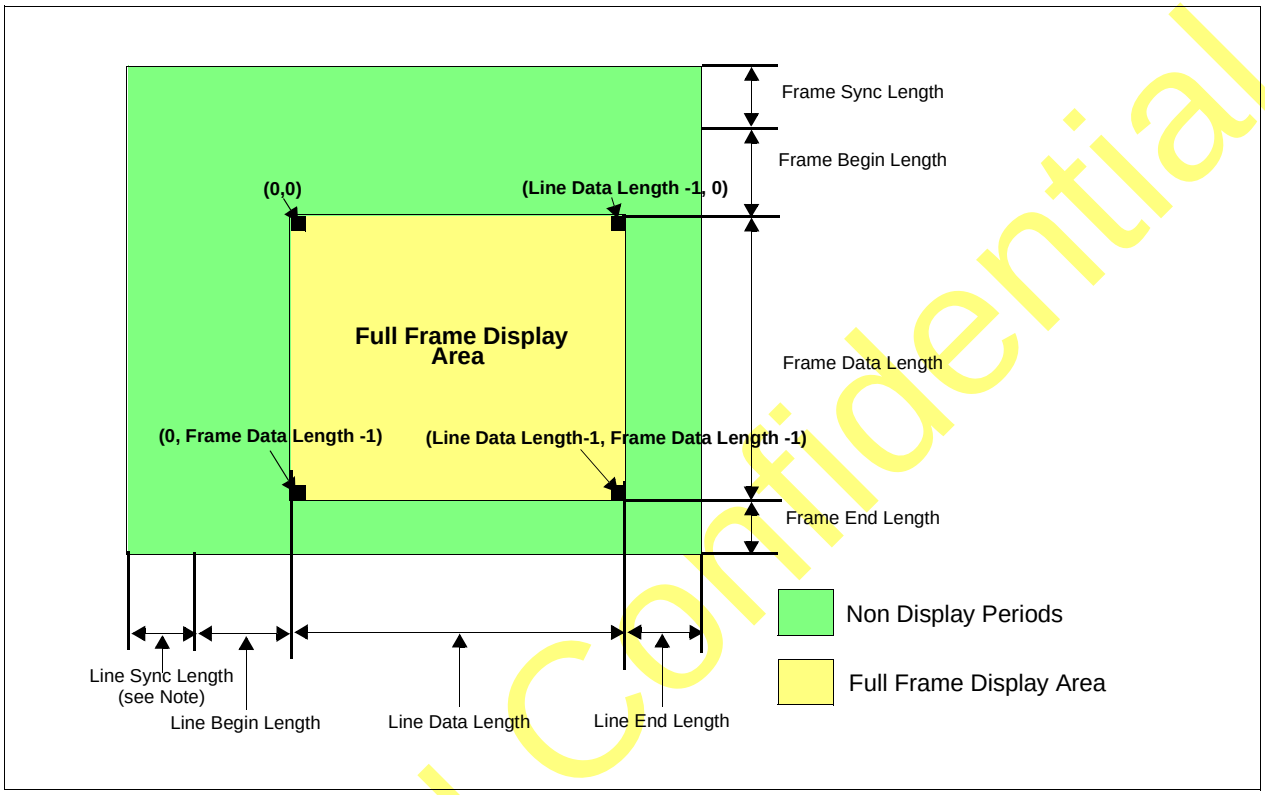


Figure 6-8: Display Timing

Note

For 8 Pixels Per Clock Cycle with Double Data Rate enabled (REG[030Ch] bit 11 = 1b and REG[030Eh] bit 10 = 1b), the line sync length should be preceded with a fixed timing of one internal pixel clock period.

6.5.1 Frame Rate Calculation Guide

The Frame Rate can be determined using the following formulas.

$$PixelClkFrequency = \frac{133Mhz}{PixelClkDivideSelected(REG[0018])}$$

$$SourceDriverClkFrequency = \frac{PixelClkFrequency}{PixelPerClockOutputSelect(REG[030C-Bit11])}$$

$$HorizontalTotalPixel = LineSyncLength + LineBeginLength + LineDataLength + LineEndLength$$

$$GateDriverGDCLKFrequency = \frac{SourceDriverClkFrequency}{HorizontalTotalPixel} MHz$$

$$VerticalTotalLines = FrameSyncLength + FrameBeginLength + FrameDataLength + FrameEndLength$$

$$FrameRate = \frac{GDCLKFrequency}{VerticalTotalLines}$$

The following shows example values for an 800x600 display.

Table 6-7 : Frame Rate Calculation Example for 800x600

Pixel Clock Divide Select	7	
Pixel Clock Frequency	16.625	MHz
SDCLK Frequency	8.3125	MHz

Internal Clock	133	MHz
Divide Selected	8	

Register Settings		
Frame Sync Length	4	
Frame Begin Length	4	
Frame End Length	5	
Frame Data Length	600	

Line Sync Length	10	
Line Begin Length	20	
Line End Length	40	
Line Data Length	800	

GDCLK High Time	230.5	SDCLKs
GDCLK Low Time	40	SDCLKs
GDCLK Frequency	30.73013	KHz

Total Lines	614	Lines
Frame Rate	50.04907	Hz

6.5.2 Interpreted Source Driver Timings

The following figure shows an example Source Driver connection using a Micronix MX860 (268 outputs per driver).

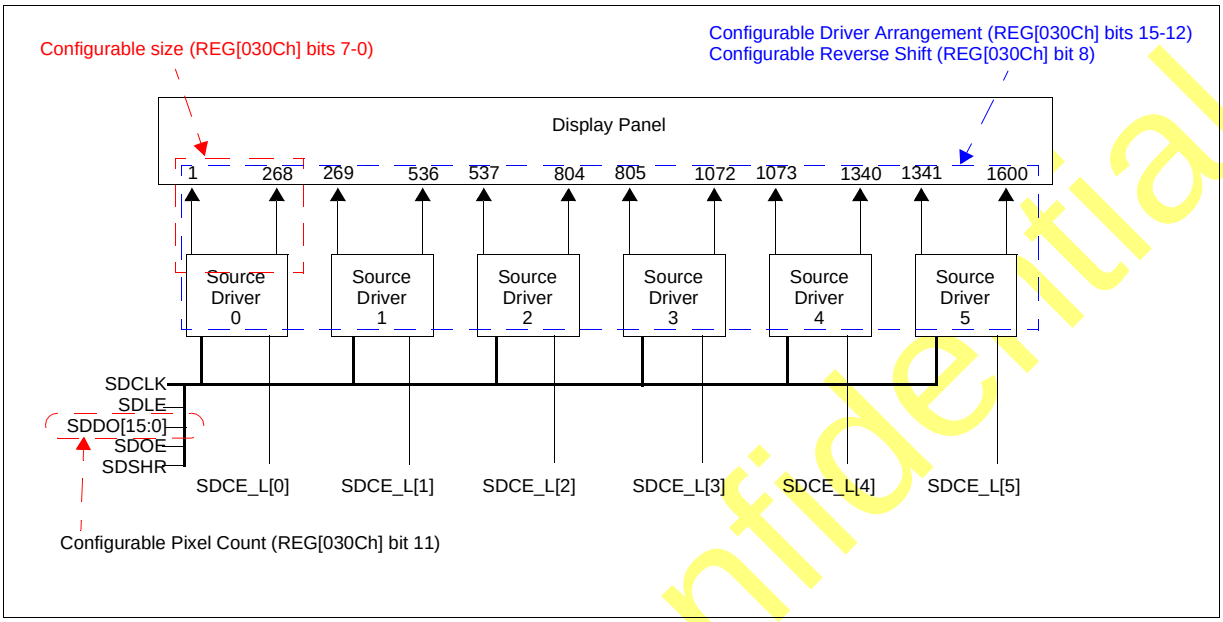


Figure 6-9: Source Driver Connection Example using MX860

Source Driver Display Timing 1: 4 Pixel per Clock Cycle

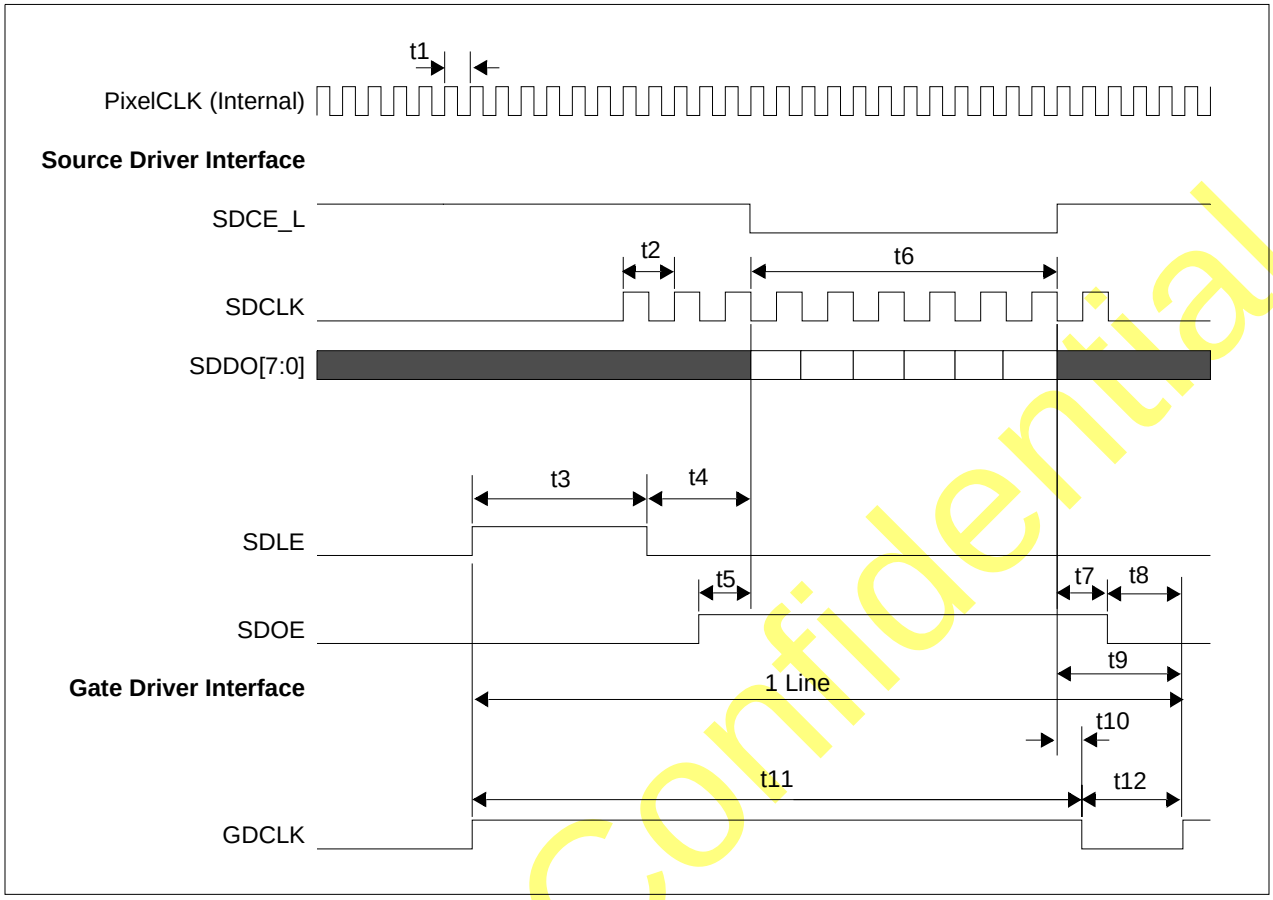


Figure 6-10: Source Driver Display Timing for 4 Pixel per clock Cycle

Table 6-8: Source Driver Display Timing for 4 Pixel Per Clock Cycle

Timing	Description	Min	Typ	Max	Units
t1	Dual Pixel Clock Period (DCLK)	11.25	Note 1	—	ns
t2	SDCLK Period for 4 Pixel per clock	22.5	2 x t1	—	ns
t3	Line Sync Length	t2	Note 2	—	ns
t4	Line Begin Length	0	Note 3	—	ns
t5	Source Driver Output Enable to Chip Enable	t2	t2	t2	ns
t6	Data Output Time (Including Padding)	4 x t2	Note 4	—	ns
t6p	Padding Data Output Time (Not shown)	0	Note 5	—	ns
t7	SDOE Deassert Time	0	Note 6	—	ns
t8	SDOE Deassert to GDCLK	—	3 x t1	—	ns
t9	Line End Length	—	t7 + t8	—	ns
t10	Gate Driver Clock Falling edge	—	t1	—	ns
t11	Gate Driver Clock High Time	—	Note 7	—	ns
t12	Gate Driver Clock Low Time	—	t9 - t10	—	ns

1. t1typ is determined by the Pixel Clock Divide.
2. t3typ = REG[0308h] bits 7-0 x t2
3. t3typ = REG[030Ah] bits 7-0 x t2
4. t6 = round up(REG[0306h] bits 12-0 ÷ (REG[030Ch] bits 7-0 x 4)) x REG[030Ch] bits 7-0 x t2
5. t6p = t6 - (REG[0306h] bits 12-0 ÷ 4 x t2)
6. t7typ = (REG[030Ah] bits 15-8 - 1) x t2 - t6p
7. t11typ = t3 + t4 + t6 + t10

Source Driver Display Timing 2: 8 Pixel per Clock Cycle (Single Data Rate)

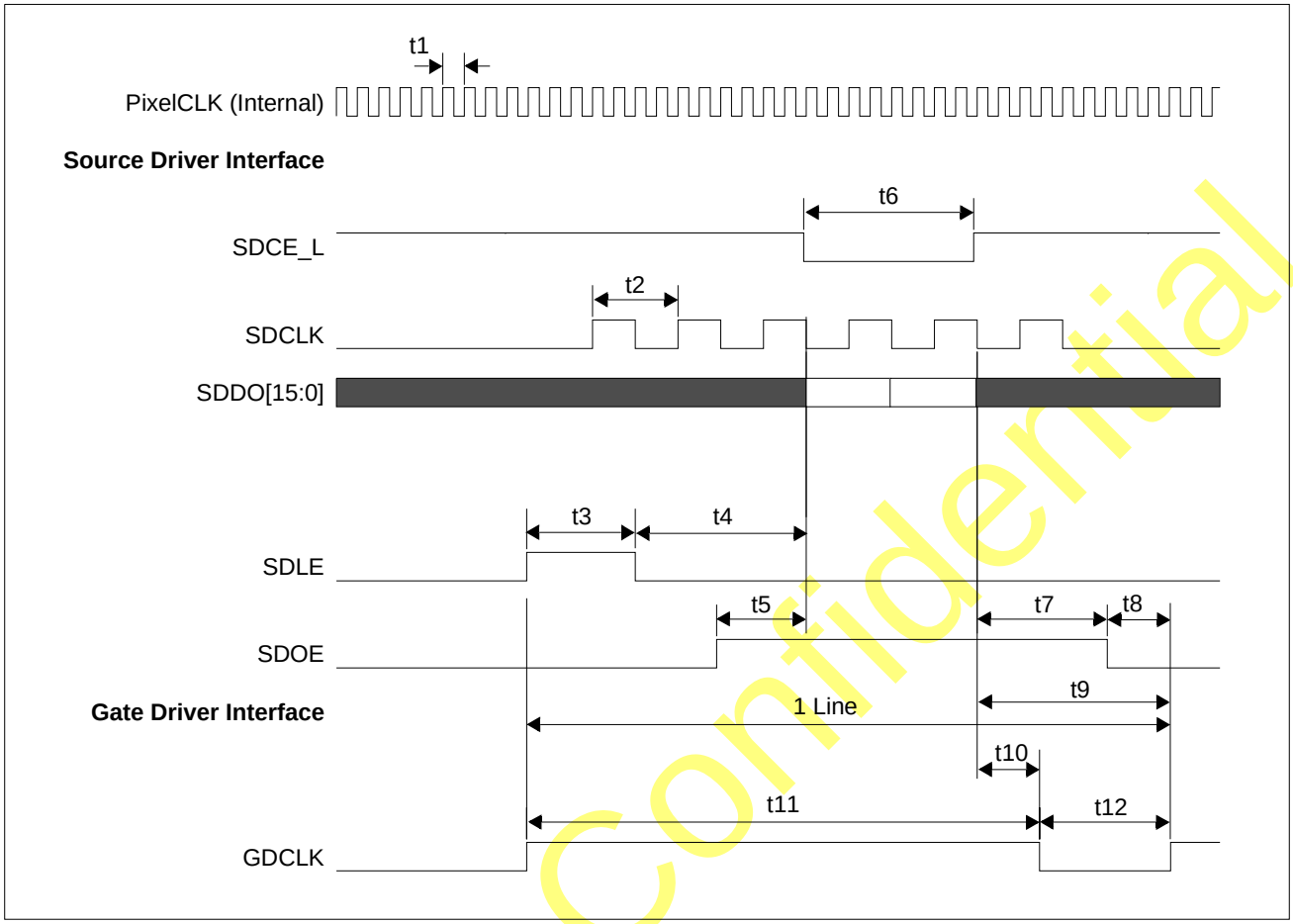


Figure 6-11: Source Driver Display Timing for 8 Pixel per clock Cycle (Single Data Rate)

Table 6-9: Source Driver Display Timing for 8 Pixel Per Clock Cycle (Single Data Rate)

Timing	Description	Min	Typ	Max	Units
t1	Dual Pixel Clock Period	11.2	Note 1	—	ns
t2	SDCLK Period for 8 Pixel per clock	45	4 x t1	—	ns
t3	Line Sync Length	t2	Note 2	—	ns
t4	Line Begin Length	0	Note 3	—	ns
t5	Source Drive Output Enable to Chip Enable	—	t2	—	ns
t6	Data Output Time (Line Data Length + Padding)	2 x t2	Note 4	—	ns
t6p	Padding Data Output Time	0	Note 5	—	ns
t7	SDOE Deassert Time	0	Note 6	—	ns
t8	SDOE Deassert to GDCLK	—	5 x t1	—	ns
t9	Line End Length	—	t7 + t8	—	ns
t10	Gate Driver Clock Falling edge	—	3 x t1	—	ns
t11	Gate Driver Clock High Time	—	Note 7	—	ns
t12	Gate Driver Clock Low Time	—	t9 - t10	—	ns

1. t1typ is determined by the Pixel Clock Divide.
2. t3typ = (REG[0308h] bits 7-0 ÷ 2) x t2
3. t4typ = (REG[030Ah] bits 7-0 ÷ 2) x t2
4. t6 = round up(REG[0306h] bits 12-0 ÷ (REG[030Ch] bits 7-0 x 4)) x REG[030Ch] bits 7-0 ÷ 2 x t2
5. t6p = t6 - (REG[0306h] bits 12-0 ÷ 8 x t2)
6. t7typ = (REG[030Ah] bits 15-8 ÷ 2 - 1) x t2 - t6p
7. t11typ = t3 + t4 + t6 + t10

Source Driver Display Timing 3: 4 Pixel per Clock Edge Output (Double Data Rate)

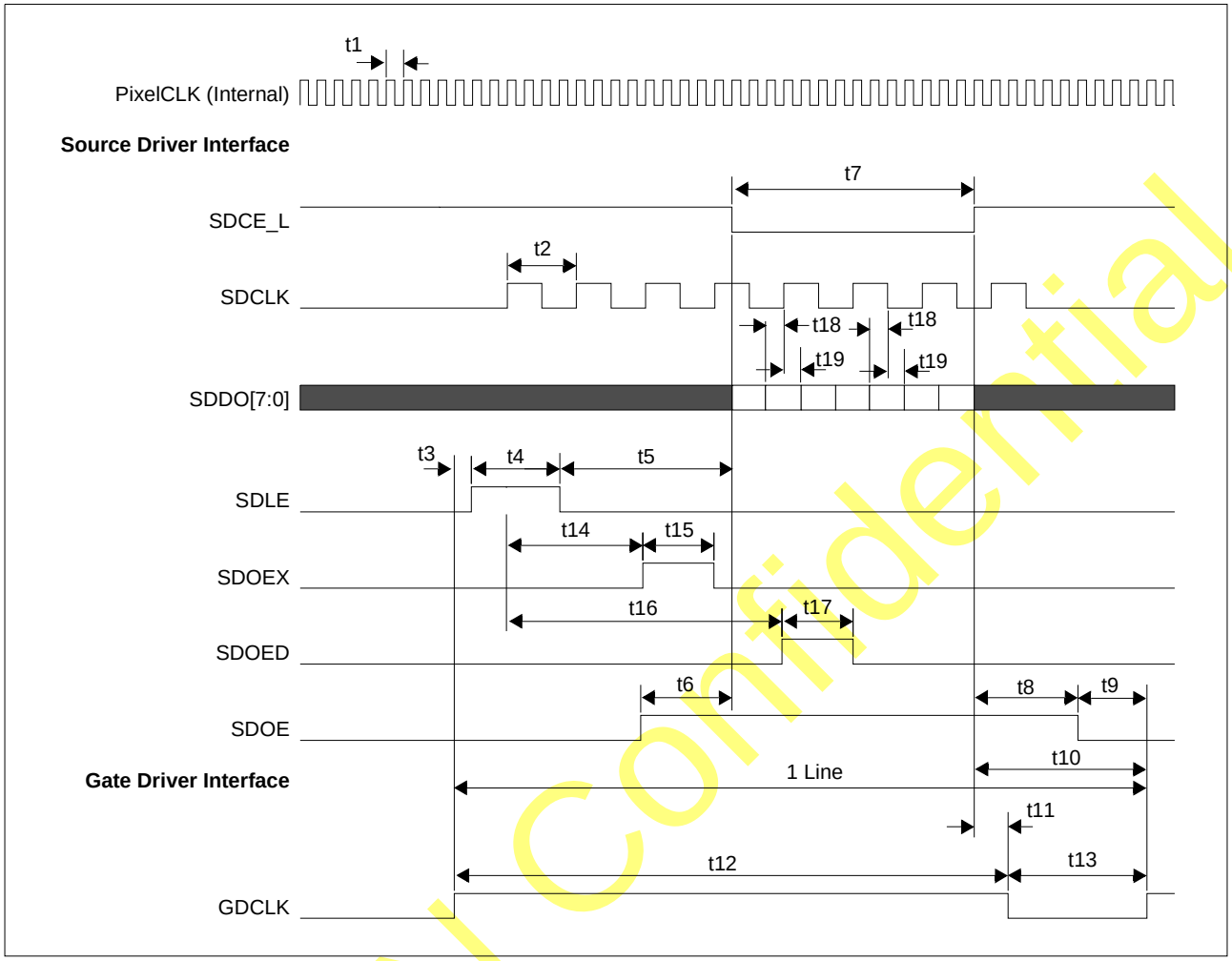


Figure 6-12: Source Driver Display Timing for 4 Pixel per Clock Edge Output

Table 6-10: Source Driver Display Timing for 4 Pixel per Clock Edge Output

Timing	Description	Min	Typ	Max	Units
t1	Dual Pixel Clock Period	11.2	Note 1	—	ns
t2	SDCLK Period for 8 Pixel per clock	45	4 x t1	—	ns
t3	Line Sync Delay	—	t1	—	ns
t4	Line Sync Length	t2	Note 2	—	ns
t5	Line Begin Length	0	Note 3	—	ns
t6	Source Driver Output Enable to Chip Enable	t2 + t1	t2 + t1	t2 + t1	ns
t7	Data Output Time (Line Data Length + Padding)	2 x t2	Note 4	—	ns
t7p	Padding Data Output Time	0	Note 5	—	ns
t8	SDOE Deassert Time	0	Note 6	—	ns
t9	SDOE Deassert to GDCLK	—	5 x t1	—	ns
t10	Line End Length	—	t8 + t9	—	ns
t11	Gate Driver Clock Falling edge	—	2 x t1	—	ns
t12	Gate Driver Clock High Time	t2	Note 7	—	ns
t13	Gate Driver Clock Low Time	t2	t10 - t11	—	ns
t14	SDOEX assert Delay	t2	Note 8	—	ns
t15	SDOEX Pulse Width	—	t2	—	ns
t16	SDOED assert Delay	t2	Note 9	—	ns
t17	SDOED Pulse Width	—	t2	—	ns
t18	Data Output Setup Time to SDCLK Edge	t1 - 2 (Note 10)	t1	t1	ns
t19	Data Output Hold Time to SDCLK Edge	t1 - 2 (Note 10)	t1	t1	ns

1. t1typ is determined by the Pixel Clock Divide.
2. t4typ = (REG[0308h] bits 7-0 ÷ 2) x t2
3. t5typ = (REG[030Ah] bits 7-0 ÷ 2) x t2
4. t7 = round up(REG[0306h] bits 12-0 ÷ (REG[030Ch] bits 7-0 x 4)) x REG[030Ch] bits 7-0 ÷ 2 x t2
5. t7p = t7 - (REG[0306h] bits 12-0 ÷ 8 x t2)
6. t8typ = (REG[030Ah] bits 15-8 ÷ 2 - 1) x t2 - t7p - t1
7. t12typ = t3 + t4 + t5 + t7 + t11
8. t14typ = REG[030Eh] bits 7-3 x t2
9. t16typ = REG[030Eh] bits 15-11 x t2
10. For PIOVDD = 3.3V, CL = 30pF.

6.5.3 Interpreted Gate Driver Timings

The following figure shows an example Gate Driver connection using a Sharp LH1692.

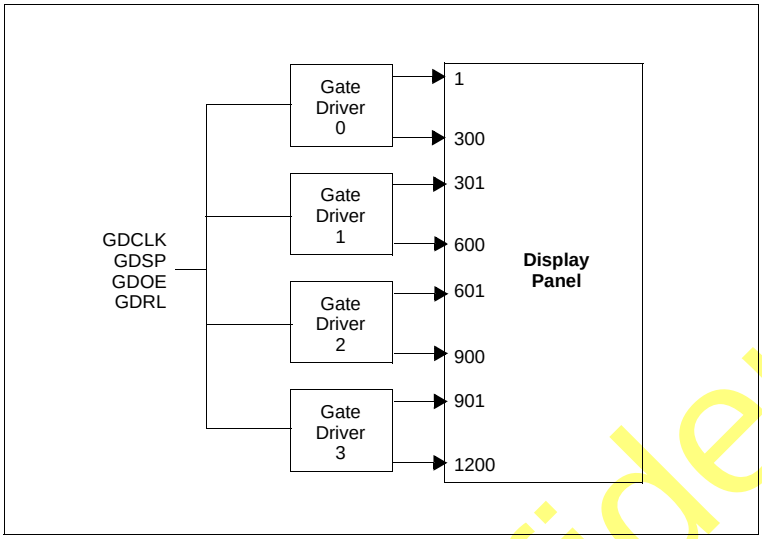


Figure 6-13: Gate Driver Connection Example using Sharp LH1692

Gate driver timings are separated into 2 sections:

- GDCLK: GDCLK is generated from Line Clock (LCLK) and Pixel Data Enable (PDEN). GDCLK is used by the gate drivers to enable gate data output.
- GDSP: GDSP is generated from GDCLK to signal a start pulse.

Gate Driver Display Timings

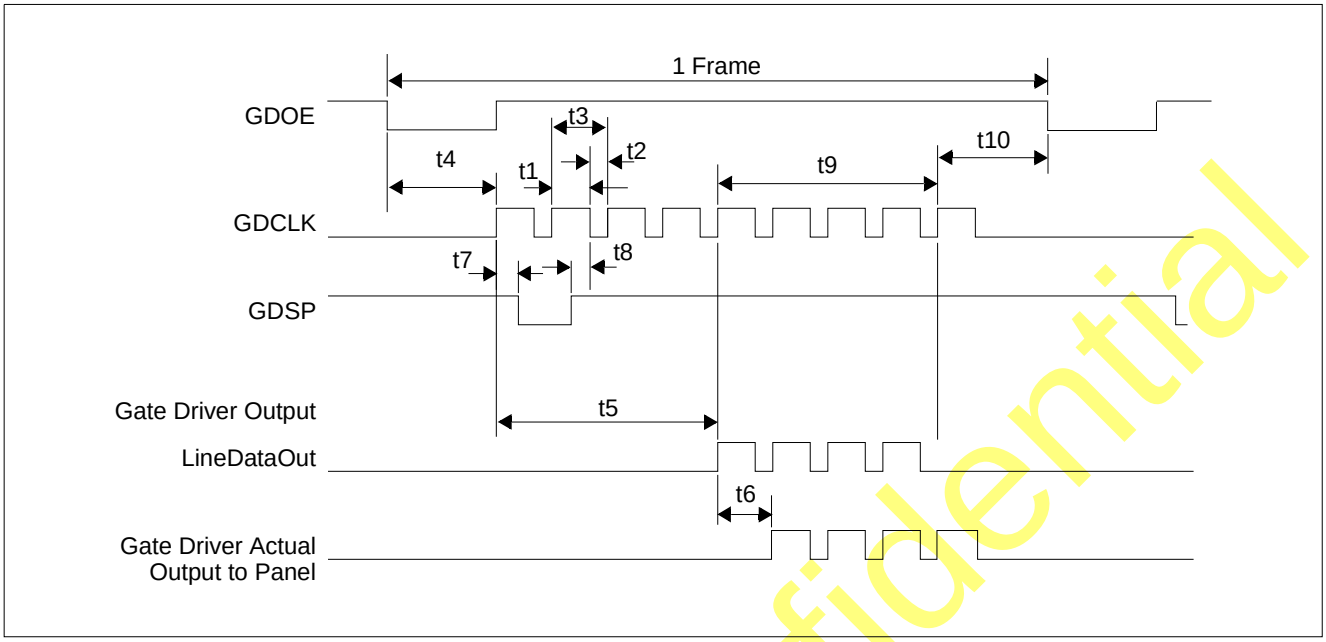


Figure 6-14: Gate Driver Timing Generation

Table 6-11: Gate Driver Timing Generation

Timing	Description	Min	Typ	Max	Units
t1	GDCLK High Level	—	Note 1	—	ns
t2	GDCLK Low Level	—	Note 2	—	ns
t3	Line Width	—	t1 + t2	—	ns
t4	Frame Sync Length	2 * t3	Note 3	—	ns
t5	Frame Begin Length	0	Note 4	—	ns
t6	Gate Driver's Actual output Valid	—	t3	—	ns
t7	GDCLK to GDSP negative edge	—	t1 ÷ 2	—	ns
t8	GDCLK to GDSP positive edge	—	t1 ÷ 2	—	ns
t9	Frame Data Length	t3	Note 5	—	ns
t10	Frame End Length	t3	Note 6	—	ns

1. See the t11 parameter in the corresponding Source Driver Timing Table.
2. See the t12 parameter in the corresponding Source Driver Timing Table.
3. t4typ = REG[0302h] bits 7-0 x t3
4. t5typ = REG[0304h] bits 7-0 x t3
5. t9typ = REG[0300h] bits 12-0 x t3
6. t10typ = (REG[0304h] bits 15-0 + 1) x t3

6.6 Power Pin Interface

6.6.1 Power Pin Transition Sequence for PWR[3:0]

The power pins PWR[3:0] operate in a cascade manner with the delay times controlled by register settings (REG[0234h] ~ REG[0238h]).

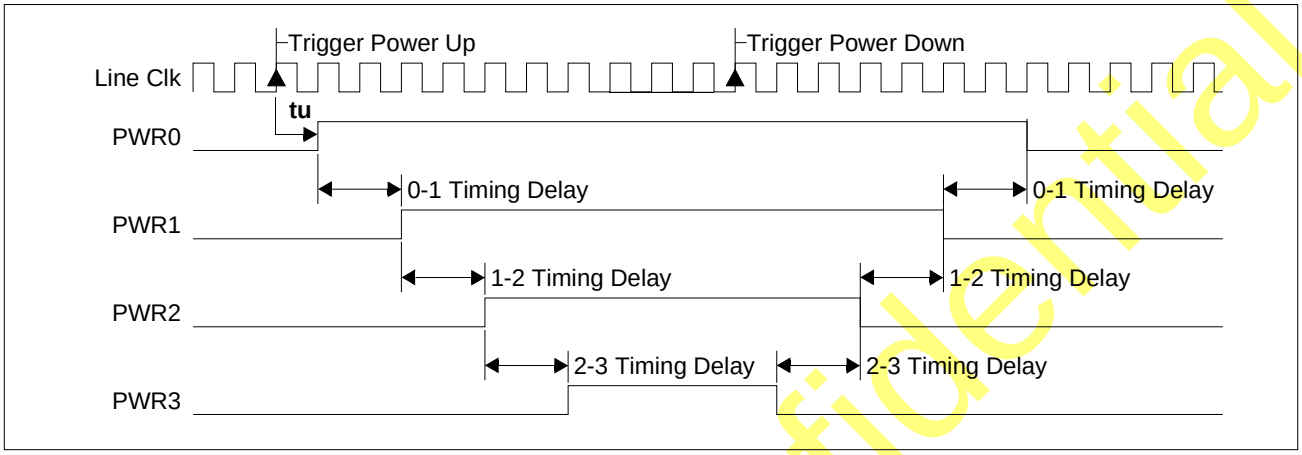


Figure 6-15: PWR[3:0] Transition Sequence

Table 6-12: PWR[3:0] Transition Timing

Symbol	Parameter	Min	Max	Units
tu	Trigger Power up to Power Pin 0 transition	0	—	ns
0-1 Timing Delay	Power pin 0 to Power pin 1 Timing Delay	1	REG[0234h]	Line Clk
1-2 Timing Delay	Power pin 1 to Power pin 2 Timing Delay	1	REG[0236h]	Line Clk
2-3 Timing Delay	Power pin 2 to Power pin 3 Timing Delay	1	REG[0238h]	Line Clk

6.6.2 Power Pin Transition Sequence for PWRCOM

The power pin PWRCOM defines the common power control. PWRCOM operations are controlled by the Display Engine update operation as shown in the following figure.

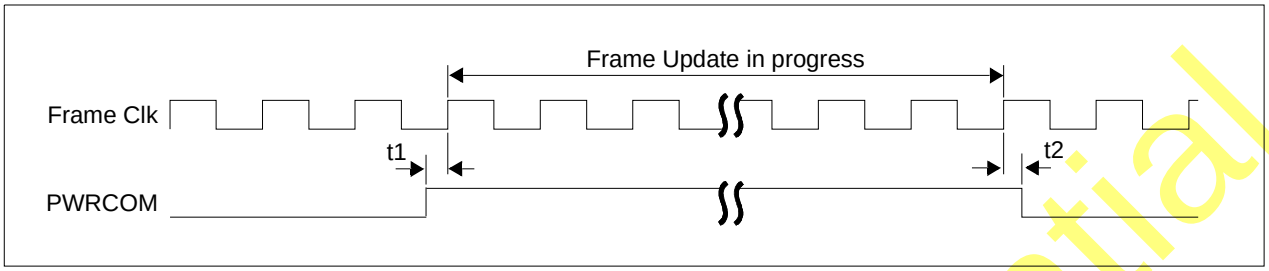


Figure 6-16: PWRCOM Transition Sequence

Table 6-13: PWRCOM Transition Timing

Symbol	Parameter	Min	Max	Units
t1	PWRCOM Active to Frame Clk	0	—	ns
t2	Frame Clk to PWRCOM Inactive	0	—	ns

Chapter 7 Clocks

7.1 Clock Descriptions

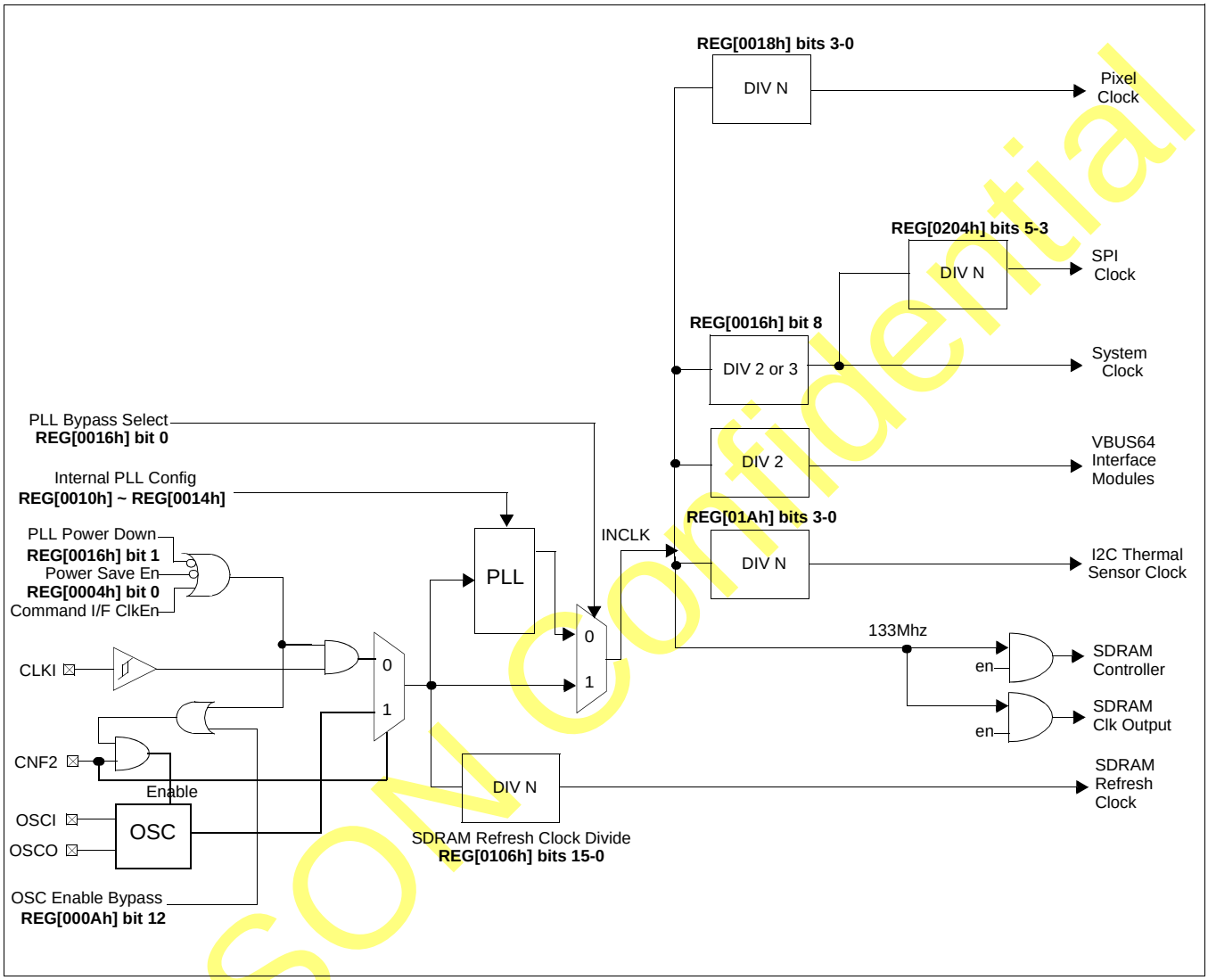


Figure 7-1: Clock Tree Diagram

Chapter 8 Power Management

8.1 Power Management State Description

The S1D13521 controller has the following power states:

- OFF State:
  Power for the S1D13521 and external SDRAM is off. Upon power-up, the Host must issue a hardware reset and an INIT_SYS_RUN command to initialize the S1D13521.
- Run State:
  The S1D13521 is ready for operation. In this state the display can be updated.
- Standby State:
  The S1D13521 is in power save mode and the SDRAM is in a Self Refresh state. The Host should not access memory while in this state.
- Sleep Mode:
  The S1D13521 is in power save mode and the SDRAM is in a Self Refresh state. Sleep Mode initiates the Power Pin power down cycles. The Host should not access memory while in this state.

The following table summarizes the S1D13521 functionality for each power state.

Table 8-1: S1D13521 Power State Functionality Summary

Power Mode	S1D13521 Controller State	S1D13521 PLL State	PWR[3:0] State	SDRAM State	SDRAM Data Retained	Power Consumption
OFF	Unknown	Unknown	Unknown	Unknown	No	NA
Run	Active All clocks active	Active	ON	Normal Operation with Auto Refresh	Yes	Low or Highest (depending on host and display activity)
Standby	Power Save Mode All module clocks gated off PLL is running	Active	ON	Self Refresh	Yes	Lower
Sleep	Power Save Mode Power Pin cycle off PLL off	Powered-Down	OFF	Self Refresh	Yes	Lowest

The following figure shows how to transition between S1D13521 power states.

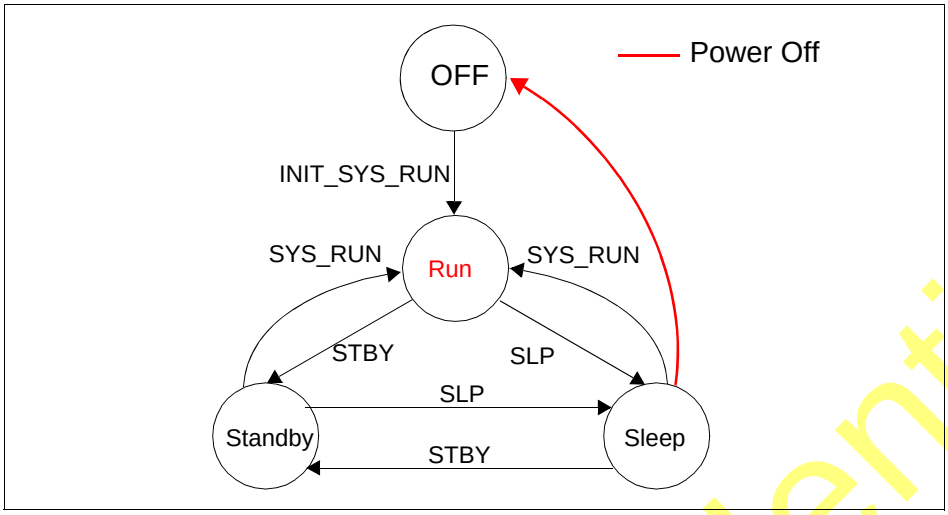


Figure 8-1: State Transition Diagram

To transition between S1D13521 power states the following steps are required.

Table 8-2: State Transition Requirements

Current State	Next State Requirements			
	Off	**Run**	**Standby**	**Sleep**
OFF	NA	1. Power on Reset 2. Run Cmd INIT_SYS_RUN	Not Possible.	Not Possible.
Run	1. Host Save Memory Contents 2. Run Cmd SLP 3. Power off	NA	1. Run Cmd STBY	1. Run Cmd SLP
Standby	1. Run Cmd SLP 2. Power off	1. Run Cmd RUN_SYS	NA	1. Run Cmd SLP
Sleep	1. Power off	1. Run Cmd RUN_SYS	1. Run Cmd STBY	NA

The estimated time required to transition between S1D13521 power states is shown in the following figure and summarized in the following table.

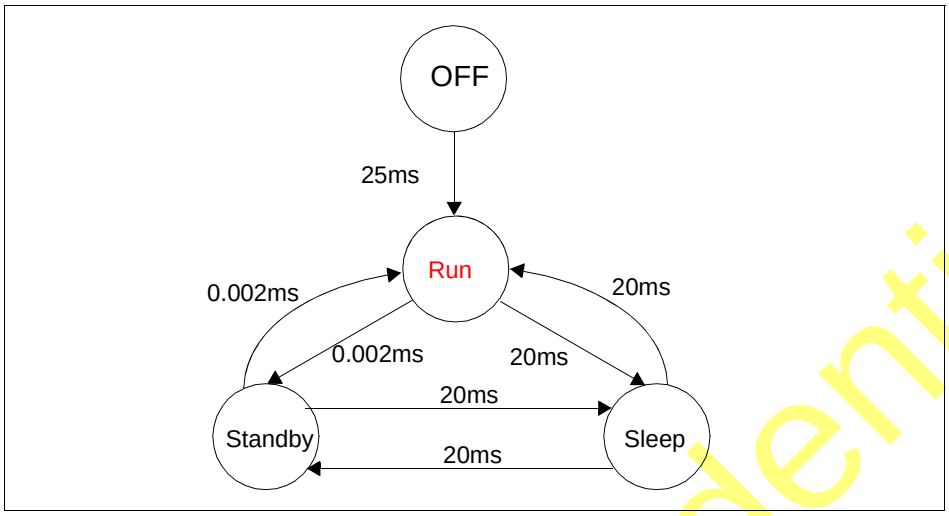


Figure 8-2: State Transition Estimated Time

Table 8-3: State Transition Estimated Time

Current State	Estimated Transition Time			
	Off	Run	Standby	Sleep
OFF	NA	25ms	NA	NA
Run	NA	NA	0.002ms	20ms
Standby	NA	0.002ms	NA	20ms
Sleep	NA	20ms	20ms	NA

Chapter 9 Host Interface

9.1 Host Cycle Sequences

9.1.1 Command and Parameter Cycle

A typical cycle consists of a Command and a variable number of parameters depending on the expected parameter count for each specific command. The following figures shows a typical cycle.

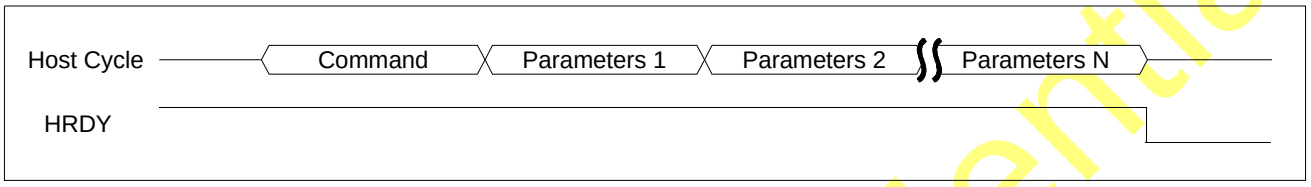


Figure 9-1: Command Mode Host Cycle Example

The HRDY line is deasserted (low) after HWE_L is deasserted (high) for the last parameter. When the sequencer is ready to accept new commands, HRDY is asserted (high) again.

9.1.2 Memory Access Combination Cycle

Commands that require Host memory access require a combination of Command/Parameter and Register Read/Write cycles. The HRDY line will deassert (low) during the memory read/write data cycles.

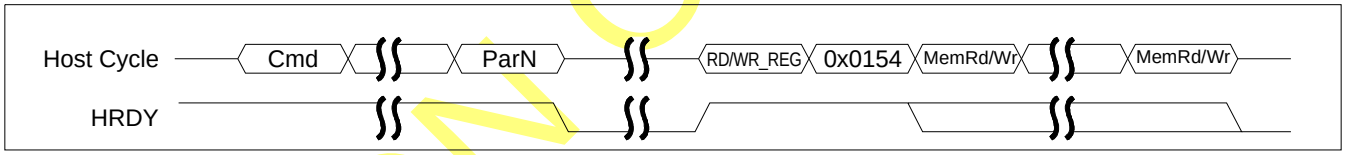


Figure 9-2: Memory Access Combination Cycle

9.2 Serial Flash Memory Contents

The S1D13521 Command Interface requires Instruction Code data to be stored in the serial flash memory from address 004h to 885h. Upon reset, the S1D13521 automatically obtains Instruction Code data from Serial Flash Memory address 004h. The Serial Flash Memory contents is shown below.

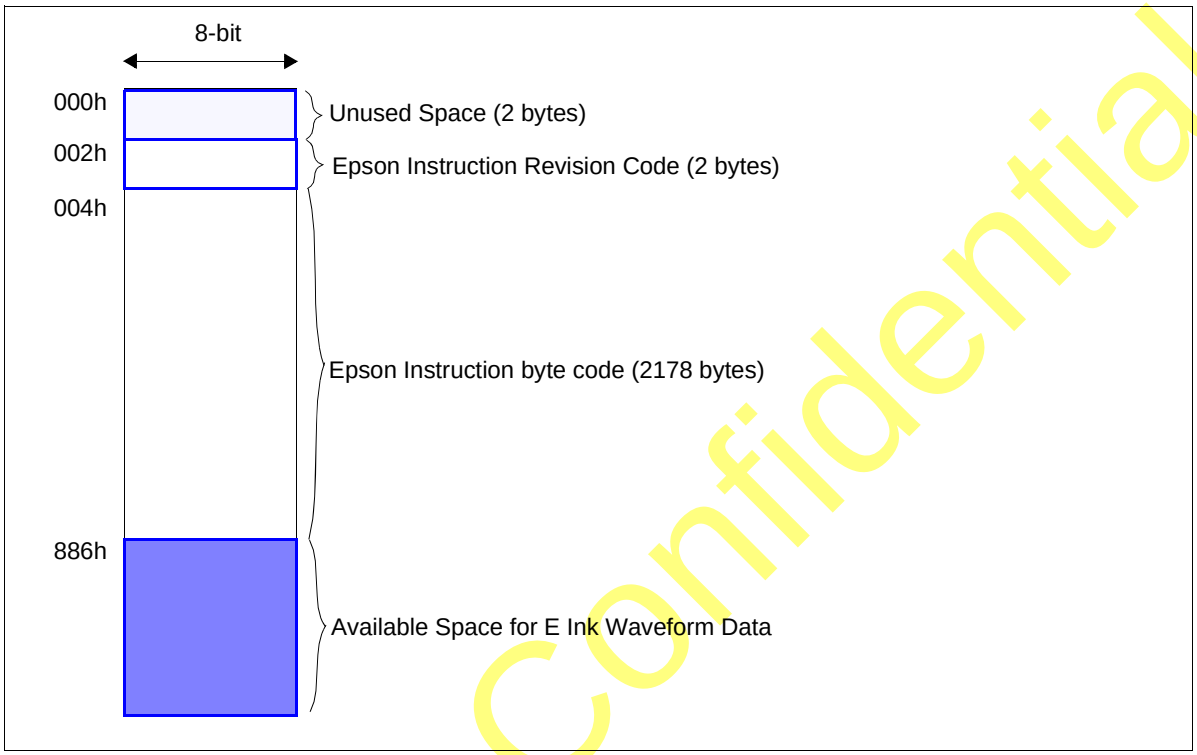


Figure 9-3: Serial Flash Memory Contents Requirement

Note
If the Serial Flash Memory is empty or contains invalid data, the RD_REG and WR_REG commands must be used to program the serial flash. For details, see 14.1.1, “Initializing and Programming a Blank Serial Flash” on page 121.

To obtain Epson Instruction byte codes and E Ink Waveform Data, contact the Epson or E Ink sales office for your area.

9.3 HRDY (Wait Line) Usage

When a command is issued, the command sequencer must execute a set of instruction codes based on the specific command. The execution time required for each command depends on the number of instruction codes that must be completed.

Once a command is issued, the host interface must not issue any new commands until HRDY is asserted High. If new Commands are inserted during this time, it will be ignored.

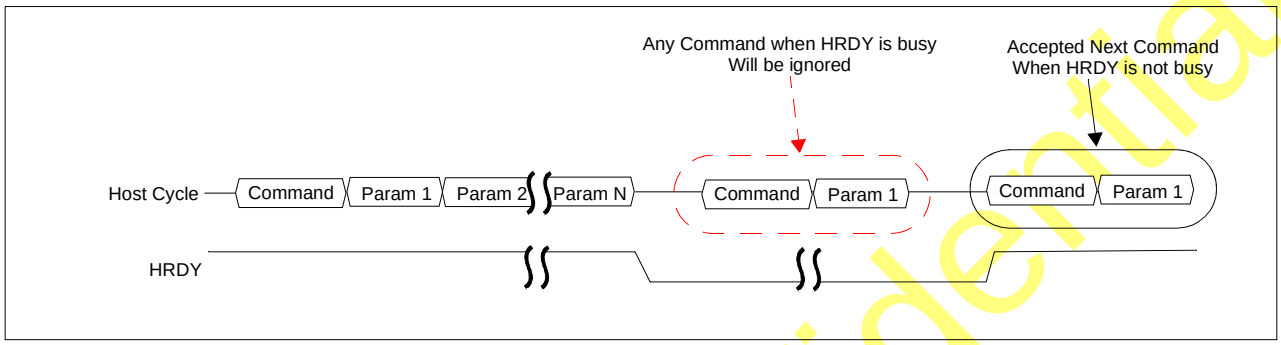


Figure 9-4: Command Mode Host Cycle Example for Host with HRDY

If the HRDY line is not used, the Host can poll the Sequence Controller Busy Status bit in REG[000Ah] bit 5 using the RD_REG command.

Note
RD_REG is implemented outside of the Sequence Controller and is specifically designed to allow execution in parallel with other command sequences. This allows polling the Sequence Controller Busy Status for Hosts that do not have HRDY.

The following figure shows a typical command/parameter sequence using Sequence Controller Busy Status polling.

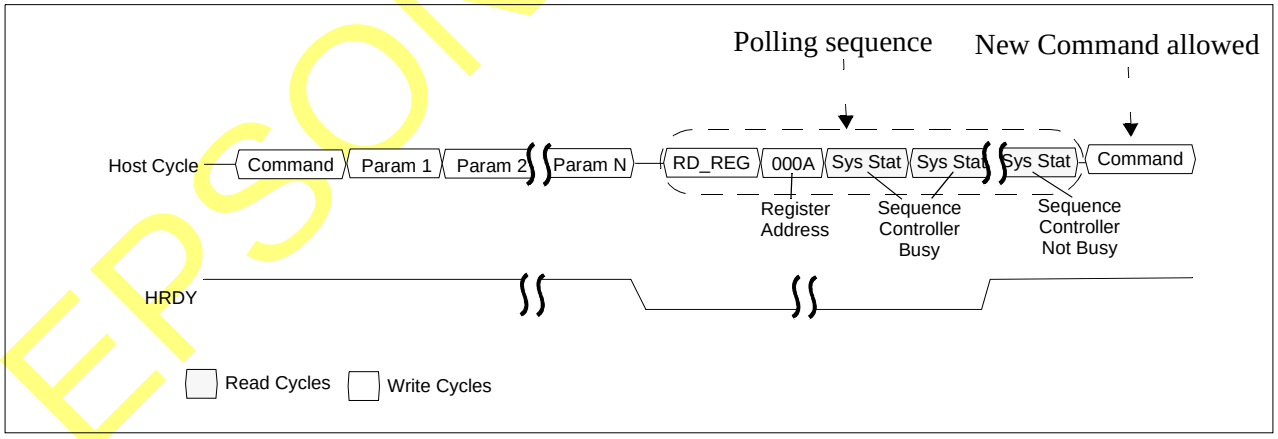


Figure 9-5: Command Mode Host Cycle Example for Host without HRDY

9.4 Command Operation

The following figure shows a typical command mode operation with parameter/data writes only.

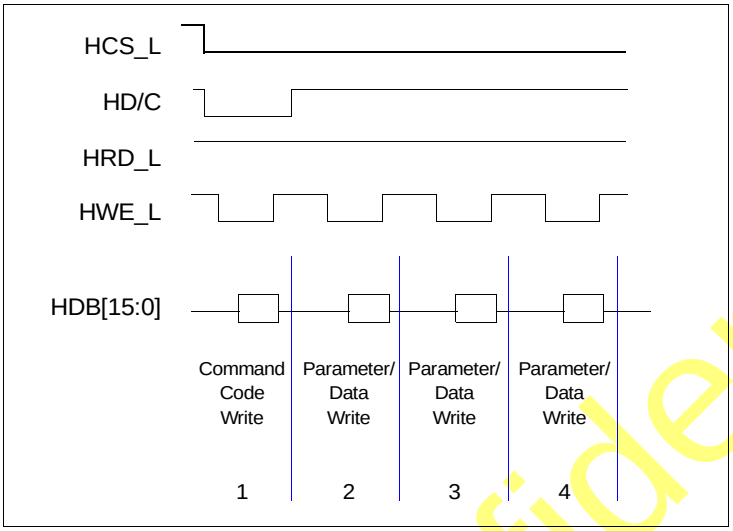


Figure 9-6: Command Mode Operation - Parameter/Data Writes Only

The following figure shows a typical command mode operation for reading register data.

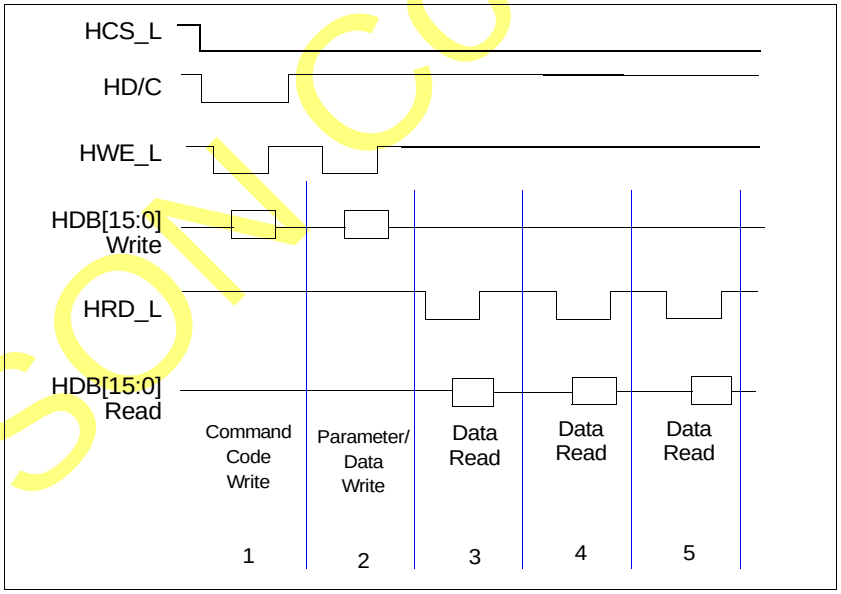


Figure 9-7: Command Mode Operation - Register Read Data

9.5 Command List

The following commands are applicable for the 16-bit Indirect Interface.

Table 9-1: Host Interface Command Summary

Code 16-bit Indirect - 2 bytes	Command	Parameters					Description
		1	2	3	4	5	
System Commands							
0x00	INIT_CMD_SET	SPI Config	SFM Adr[15:0]	SFM[23:16]	—	—	Initialize Instruction code from Specific Serial Flash Address
0x01	INIT_PLL_STBY	PLL Config0	PLL Config1	PLL Config2	—	—	Initialize PLL and Go Into Standby Mode
0x02	RUN_SYS	—	—	—	—	—	Run System using PLL
0x04	STBY	—	—	—	—	—	Go to Standby Mode
0x05	SLP	—	—	—	—	—	Go to Sleep Mode
0x06	INIT_SYS_RUN	—	—	—	—	—	Initialize System and Go into Run State
0x07	INIT_SYS_STBY	—	—	—	—	—	Initialize System and Go into Standby State
0x08	INIT_SDRAM	SDRAMCFG0	SDRAMCFG1	SDRAMCFG2	SDRAMCFG3	—	Initialize SDRAM
0x09	INIT_DSPE_CFG	HSIZE	VSIZE	SDRVCFG	GDRVCFG	LUT Index Format CFG	Initialize Display Engine
0x0A	INIT_DSPE_TMG	Frame Sync CFG	Frame Begin/End CFG	Line Sync CFG	Line Begin/End CFG	Pixel Clock CFG	Initialize Driver Timings
0x0B	INIT_ROTMODE	ROTMODE	—	—	—	—	Initialize Rotation Mode Timings
Register and Memory Access Commands							
0x10	RD_REG	REGADDR[15:0]	RDATA[15:0]	—	—	—	Read Register **Refer to detailed descriptions**
0x11	WR_REG	REGADDR[15:0]	WDATA[15:0]	—	—	—	Write Register **Refer to detailed descriptions**
0x12	RD_SFM	—	—	—	—	—	Trigger Serial Flash Read Operation
0x13	WR_SFM	WDATA[15:0]	—	—	—	—	Trigger Serial Flash Write Operation
0x14	END_SFM	—	—	—	—	—	END SFM Operation
Burst Access Commands							
0x1C	BST_RD_SDR	MA[15:0]	MA[25:16]	BC[15:0]	BC[25:16]	—	Start Burst Read SDRAM Memory
0x1D	BST_WR_SDR	MA[15:0]	MA[25:16]	BC[15:0]	BC[25:16]	—	Start Burst Write SDRAM Memory
0x1E	BST_END_SDR	—	—	—	—	—	Burst End
Image Loading Commands							
0x20	LD_IMG	ARG[15:0]	—	—	—	—	Load Image Full
0x22	LD_IMG_AREA	ARG[15:0]	XSTART[11:0]	YSTART[11:0]	WIDTH[12:0]	HEIGHT[12:0,	Load Image Area With parameters
0x23	LD_IMG_END	—	—	—	—	—	Load Image End
0x24	LD_IMG_WAIT	—	—	—	—	—	Load Image Wait End
0x25	LD_IMG_SETADR	MA[15:0]	MA[25:16]	—	—	—	Set Load Image Manual Address
0x26	LD_IMG_DSPEADR	—	—	—	—	—	Set Load Image to use Display Engine's Address
Polling Commands							
0x28	WAIT_DSPE_TRG	—	—	—	—	—	Wait For Display Engine Trigger Done
0x29	WAIT_DSPE_FREND	—	—	—	—	—	Wait For Display Engine Frame End
0x2A	WAIT_DSPE_LUTFREE	—	—	—	—	—	Wait For Display Engine At least 1 LUT is Free
0x2B	WAIT_DSPE_MLUTFREE	LUT Mask [15:0]	—	—	—	—	Wait For Display Engine At least 1 Masked LUT is Free

Table 9-1: Host Interface Command Summary

Code 16-bit Indirect - 2 bytes	Command	Parameters					Description
		1	2	3	4	5	
Waveform Update Commands							
0x30	RD_WFM_INFO	MA[15:0]	MA[23:16]	—	—	—	Read Waveform Information
0x32	UPD_INIT	—	—	—	—	—	Update Buffer Initialize
0x33	UPD_FULL	ARG[15:0]	—	—	—	—	Update Buffer Full
0x34	UPD_FULL_AREA	ARG[15:0]	XSTART[11:0]	YSTART[11:0]	WIDTH[12:0]	HEIGHT[12:0]	Update Buffer Full Area
0x35	UPD_PART	ARG[15:0]	—	—	—	—	Update Buffer Partial
0x36	UPD_PART_AREA	ARG[15:0]	XSTART[11:0]	YSTART[11:0]	WIDTH[12:0]	HEIGHT[15:0]	Update Buffer Partial Area
0x37	UPD_GDRV_CLR	—	—	—	—	—	Gate Driver Clear Command
0x38	UPD_SET_IMGADR	ADR[15:0]	ADR[25:16]	—	—	—	Set Image Buffer Start Address
0x38-0x3F	**Reserved**	—	—	—	—	—	Reserved

9.6 Host Interface Command Descriptions

The Command Sequencer supports up to 64 available commands. The first 8 commands (command codes 0x00 ~ 0x07) turn on the temporary clock enable until the command sequence has finished. This feature is for implementing commands (i.e. INIT_CMD_SET, INIT_PLL, SLP) where the S1D13521 is, or will be, in SLP mode before or after the command sequence command is completed. In SLP mode, the input clock is gated off in order to minimize power consumption. However, a clock is needed for the Sequencer Controller logic while it is operating.

Three commands are reserved and cannot be re-programmed.

- 0x00 - INIT_CMD_SET
- 0x10 - RD_REG
- 0x11 - WR_REG

These commands are hard-coded in logic allowing them to operate even before the pre-programmed command sequence is loaded into the chip. RD_REG (which can be executed in parallel with the Sequence Controller) can poll the busy status of the Sequence Controller to determine when the previous command sequence has finished. This is useful for Hosts that have no HRDY support.

Note
Although the RD_REG and WR_REG commands can be executed in parallel with the Sequence Controller, register reads/writes are not recommended while the Sequence Controller is in operation. The exception to this rule is polling the busy status bit.

9.6.1 INIT_CMD_SET (0x00 + 3 parameters)

This command initializes the Command Interface instruction table and codes. The parameters setup the SPI operating mode and the Serial Flash Memory address where the instruction table and codes are stored.

Parameter Count = 3

Parameter 1 (Recommended Setting = 0x0041)							
n/a							
15	14	13	12	11	10	9	8
SPI Flash Access Mode Select	SPI Flash Read Command Select	SPI Flash Clock Divide Select bits 2-0			SPI Flash Clock Phase Select	SPI Flash Clock Polarity Select	SPI Flash Enable
7	6	5	4	3	2	1	0

For a detailed description of the bits in Parameter 1, see the REG[0204h] bit descriptions in A.3.6, “SPI Flash Memory Interface” on page 184.

Parameter 2							
Serial Flash Memory Address Select bits 15-8							
15	14	13	12	11	10	9	8
Serial Flash Memory Address Select bits 7-0							
7	6	5	4	3	2	1	0

Parameter 3							
n/a							
15	14	13	12	11	10	9	8
Serial Flash Memory Address Select bits 23-16							
7	6	5	4	3	2	1	0

Parameter 3 bits 7-0

Parameter 2 bits 15-0 Serial Flash Memory Address Select bits [23:0]

These bits specify the memory start address in the Serial Flash Memory where the Instruction Codes are located.

9.6.2 INIT_PLL_STBY (0x01 + 3 parameters)

This command initializes the PLL and sets the S1D13521 into Standby Mode. PLL Configuration is programmed using the three input parameters. When PLL Lock is asserted, this command sequence is completed.

Functions performed:
1. Program PLL registers
2. Disable PLL Power Down (REG[0016h]) to 0001h
3. Wait for PLL Lock
4. Program State Status register to Standby Mode (REG[000Ah] bits 11-10 = 2h)
5. Turn On Power Save Mode (REG[0006h] bit 0 = 1b)

Next Command Blocking: Yes

Parameter 1

15	14	13	12	11	10	9	8
Reserved							
7	6	5	4	3	2	1	0
n/a		M-Divider bits 5-0					

Parameter 2

15	14	13	12	11	10	9	8
VCO Kv Setting bits 3-0				Reserved			
7	6	5	4	3	2	1	0
Reserved				n/a		Reserved	

Parameter 3

15	14	13	12	11	10	9	8
n/a	Reserved						
7	6	5	4	3	2	1	0
NN Setting bits 3-0				Reserved		Reserved	

For a detailed description of the bits in Parameters 1-3, see the REG[0010h] ~ REG[0014h] register descriptions in A.3.2, “Clock Configuration Registers” on page 166.

9.6.3 RUN_SYS (0x02 + 0 parameters)

This command places the S1D13521 into normal operation mode. This includes enabling the PLL and/or disabling power save mode (i.e. removing the S1D13521 from Standby or Sleep mode).

Functions performed:
1. Disable PLL Power Down (if not disabled already)
2. Wait for PLL Lock (if step 1 is valid)
3. Disable Power Save Mode (REG[0006h] bit 0 <= 0)
4. Trigger Power Pin - On Sequence
5. Trigger SDRAM - Exit Self-Refresh
6. Wait for SDRAM - Ensure Self-Refresh is exited and Power Pin sequence is done
7. Program State Status Register (REG[000Ah] bits 11-10 to 1h (Normal Operation)

Next Command Blocking: Yes

9.6.4 STBY (0x04 + 0 parameters)

This command places the S1D13521 into Standby mode. To wake up from Standby mode, use the RUN_SYS command.

Functions performed:
1. Wait for all modules to be idle (HMEM, I2C, SPI, PWR, 3-wire, SDRAM, and DSPE)
2. Power Pin (Enter Off State)
3. SDRAM (Enter Self-Refresh Mode)
4. SDRAM (Wait for Self-Refresh Mode Entered) and Power Pin (Wait for Off State Entered)
5. Program State Status register to Standby Mode (REG[000Ah] bits 11-10 = 2h)
6. Power Save (Enable)

Next Command Blocking: Yes

9.6.5 SLP (0x05 + 0 parameters)

This command places the S1D13521 into Sleep mode. Sleep mode differs from Standby mode in that the PLL is powered down. To wake up from Sleep mode, use the RUN_SYS command.

Functions performed:
1. Wait for all modules to be idle (HMEM, I2C, SPI, PWR, 3-wire, SDRAM, and DSPE)
2. Power Pin (Enter Off State)
3. SDRAM (Enter Self-Refresh Mode)
4. SDRAM (Wait for Self-Refresh Mode Entered)
5. Power Pin (Wait for Off State Entered)
6. Power Save (Enable)
7. PLL Power Down (Enable Power Down)

Next Command Blocking: Yes

9.6.6 INIT_SYS_RUN (0x06 + 0 parameters)

This command initializes the S1D13521 according to the requirements of the customer.

Functions performed:
1. Configure PLL (PLLM = 3
2. PLL RUN
3. PLL (Wait Lock)
4. Disable Power Save Mode
5. SDRAM Init (according to customer setting)
6. DSPE Init (according to customer setting)
7. PWRPIN Init
8. Wait SDRAM Init done and PWRPIN POWER-ON
9. Power State (Write 0x1)

Next Command Blocking: Yes

9.6.7 INIT_SYS_STBY (0x07 + 0 parameters)

This command initializes the S1D13521 according to the requirements of the customer and places the S1D13521 into Standby mode.

Functions performed:
1. Configure PLL (PLLM = 3
2. PLL RUN
3. PLL (Wait Lock)
4. Disable Power Save Mode
5. SDRAM Init (according to customer setting)
6. DSPE Init (according to customer Setting)
7. PWRPIN Init
8. SDRAM Enter Self Refresh Mode, Power-Pin Off State
9. Power State (Write 0x2)
10. Enter Power Save Mode.

Next Command Blocking: Yes

9.6.8 INIT_SDRAM (0x08 + 4 parameters)

This command initializes the SDRAM.

Functions performed:
1. Setup the SDRAM registers using the specified parameters
2. Initialize the SDRAM
3. Wait for the SDRAM Initialize to complete

Next Command Blocking: Yes

Parameter 1

SDRAM Power Down Disable	SDRAM Refresh Cycle Time bits 1-0			SDRAM Refresh Rate bits 1-0		SDRAM Row Active Time bits 1-0	
15	14	13	12	11	10	9	8
16-bit SDRAM Enable	SDRAM tRP Latency Select	SDRAM tRCD Latency Select	SDRAM tCL Latency Select	n/a	SDRAM Column Address Count bits 1-0		SDRAM Burst Type Select
7	6	5	4	3	2	1	0

For a detailed description of the bits in Parameter 1, see the REG[0100h] bit descriptions in A.3.4, “Memory Controller Configuration” on page 171.

Parameter 2

SDRAM Refresh Clock Divide Select bits 15-8							
15	14	13	12	11	10	9	8
SDRAM Refresh Clock Divide Select bits 7-0							
7	6	5	4	3	2	1	0

For a detailed description of the bits in Parameter 2, see the REG[0106h] bit descriptions in A.3.2, “Clock Configuration Registers” on page 166.

Parameter 3							
n/a							
15	14	13	12	11	10	9	8
Reserved	n/a	SDRAM Read Data Sampling Select	SDRAM Read Data Sampling Clock Invert Enable	Reserved	Reserved		
7	6	5	4	3	2	1	0

Parameter 3 must be set to 80h.

Parameter 4							
n/a	SDRAM Driver Strength bits 1-0		Temperature Compensated Self Refresh bits 1-0		Partial Array Self Refresh bits 2-0		
15	14	13	12	11	10	9	8
n/a					SDRAM Size bits 1-0		Extended Mode Register Program on Initialization Enable
7	6	5	4	3	2	1	0

For a detailed description of the bits in Parameter 4, see the REG[010Ah] bit descriptions in A.3.2, “Clock Configuration Registers” on page 166.

9.6.9 INIT_DSPE_CFG (0x09 + 5 parameters)

This command initializes the Display Engine.

Functions performed:
1. Initializes the Display Engine according to the specified parameters
2. Set REG[032Ch] to 0x0400, Area Size Mode Enabled

Parameter 1							
n/a			Line Data Length bits 12-8				
15	14	13	12	11	10	9	8
Line Data Length bits 7-0							
7	6	5	4	3	2	1	0

For a detailed description of the bits in Parameter 1, see the REG[0306h] bit descriptions in A.3.13, “Display Engine: Display Timing Configuration” on page 205.

Parameter 2							
n/a			Frame Data Length bits 12-8				
15	14	13	12	11	10	9	8
Frame Data Length bits 7-0							
7	6	5	4	3	2	1	0

For a detailed description of the bits in Parameter 2, see the REG[0300h] bit descriptions in A.3.13, “Display Engine: Display Timing Configuration” on page 205.

Parameter 3							
Source Driver Chip Enable Start bits 3-0				Source Driver Pixel Output Count Select	Source Driver Chip Enable Reverse	Source Driver Output Reverse	Source Driver Shift Right
15	14	13	12	11	10	9	8
Source Driver Output Size Select bits 7-0							
7	6	5	4	3	2	1	0

For a detailed description of the bits in Parameter 3, see the REG[030Ch] bit descriptions in A.3.14, “Display Engine: Driver Configurations” on page 208.

Parameter 4							
Source Driver SDOED Delay bits 4-0					Source Driver Double Data Rate Enable	Source Driver Swap Padding Pixels	Source Driver Early SDOE Assert Disable
15	14	13	12	11	10	9	8
Source Driver SDOEX Delay bits 4-0					n/a	Gate Driver Right/Left Select	Gate Driver Start Pulse Polarity
7	6	5	4	3	2	1	0

For a detailed description of the bits in Parameter 4, see the REG[030Eh] bit descriptions in A.3.14, “Display Engine: Driver Configurations” on page 208.

Parameter 5							
Display Engine Software Reset (WO)	n/a						
15	14	13	12	11	10	9	8
LUT Auto Select Enable	Auto Waveform Mode Select Enable	n/a			LUT Index Format Select bits 2-0		
7	6	5	4	3	2	1	0

For a detailed description of the bits in Parameter 5, see the REG[0330h] bit descriptions in A.3.17, “Display Engine: Control/Trigger Registers” on page 216.

9.6.10 INIT_DSPE_TMG (0x0A + 5 parameters)

This command initializes the display timing information.

Functions performed:
1. Initialize the Display Engine display timing according to parameters 1-4
2. Initialize the Pixel Clock according to parameter 5

Parameter 1							
n/a							
15	14	13	12	11	10	9	8
Frame Sync Length bits 7-0							
7	6	5	4	3	2	1	0

Parameter 2							
Frame End Length bits 7-0							
15	14	13	12	11	10	9	8
Frame Begin Length bits 7-0							
7	6	5	4	3	2	1	0

For a detailed description of the bits in Parameters 1-2, see the REG[0302h] ~ REG[0304h] register descriptions in A.3.13, “Display Engine: Display Timing Configuration” on page 205.

Parameter 3							
n/a							
15	14	13	12	11	10	9	8
Line Sync Length bits 7-0							
7	6	5	4	3	2	1	0

Parameter 4							
Line End Length bits 7-0							
15	14	13	12	11	10	9	8
Line Begin Length bits 7-0							
7	6	5	4	3	2	1	0

For a detailed description of the bits in Parameter 3-4, see the REG[0308h] ~ REG[030Ah] register descriptions in A.3.13, “Display Engine: Display Timing Configuration” on page 205.

Parameter 5							
n/a							
15	14	13	12	11	10	9	8
n/a			Pixel Clock Divide Disable	Pixel Clock Divide Select bits 3-0			
7	6	5	4	3	2	1	0

For a detailed description of the bits in Parameter 5, see the REG[0018h] bit descriptions in A.3.2, “Clock Configuration Registers” on page 166.

9.6.11 INIT_ROTMODE (0x0B + 1 parameter)

This command initializes the S1D13521 Rotation Mode

Functions performed:
1. Set REG[032Ch] bits 9-8 with the specified Rotation Mode
2. Set REG[0140h] bits 9-8 with the specified Rotation Mode

Parameter 1							
n/a						Rotation Mode bits 1-0	
15	14	13	12	11	10	9	8
n/a							
7	6	5	4	3	2	1	0

9.6.12 RD_REG (0x10 + 2 parameters)

This command initiates a low level register read from the address specified by parameter 1. The returned data value is available in parameter 2.

Parameter 1							
Register Address bits 15-8							
15	14	13	12	11	10	9	8
Register Address bits 7-0							
7	6	5	4	3	2	1	0

Parameter 2							
Register Read Data bits 15-8							
15	14	13	12	11	10	9	8
Register Read Data bits 7-0							
7	6	5	4	3	2	1	0

9.6.13 WR_REG (0x11 + 2 parameters)

This command initiates a low level register write of the data specified by parameter 2 to the address specified by parameter 1..

Parameter 1							
Register Address bits 15-8							
15	14	13	12	11	10	9	8
Register Address bits 7-0							
7	6	5	4	3	2	1	0

Parameter 2							
Register Write Data bits 15-8							
15	14	13	12	11	10	9	8
Register Write Data bits 7-0							
7	6	5	4	3	2	1	0

9.6.14 RD_SFM (0x12 + 0 parameters)

This command initiates a low level read from the Serial Flash Memory.

9.6.15 WR_SFM (0x13 + 1 parameter)

This command initiates low level write of the data specified by parameter 1 to the Serial Flash Memory.

Parameter 1							
15	14	13	12	11	10	9	8
Serial Flash Memory Write Data bits 7-0							
7	6	5	4	3	2	1	0

9.6.16 END_SFM (0x14 + 0 parameters)

This command ends a low level operation to/from the Serial Flash Memory.

9.6.17 BST_RD_SDR (0x1C + 4 parameters)

This command starts a memory burst read operation.

Functions performed:
1. End Previous Host Memory access operation if currently active.
2. Setup Read Mode and Raw Access Mode on REG[0140h]
3. Setup Raw Address
4. Setup Burst Size
5. Trigger Start and Wait for Ready..

Parameter 1							
Host Raw Memory Access Address bits 15-8							
15	14	13	12	11	10	9	8
Host Raw Memory Access Address bits 7-0							
7	6	5	4	3	2	1	0

Parameter 2							
Reserved						Host Raw Memory Access Address bits 25-24	
15	14	13	12	11	10	9	8
Host Raw Memory Access Address bits 23-16							
7	6	5	4	3	2	1	0

Parameter 3							
Host Raw Memory Access Count bits 15-8							
15	14	13	12	11	10	9	8
Host Raw Memory Access Count bits 7-0							
7	6	5	4	3	2	1	0

Parameter 4							
Reserved						Host Raw Memory Access Count bits 25-24	
15	14	13	12	11	10	9	8
Host Raw Memory Access Count bits 23-16							
7	6	5	4	3	2	1	0

For a detailed description of the bits in Parameters 1-4, see the REG[0144h] ~ REG[014Ah] register descriptions in A.3.5, “Host Interface Memory Access Configuration” on page 177.

9.6.18 BST_WR_SDR (0x1D + 4 parameters)

This command starts a memory burst write operation.

Functions performed:
1. End Previous Host Memory access operation if currently active.
2. Setup Write Mode and Raw Access Mode on REG[0140h]
3. Setup Raw Address
4. Setup Burst Size
5. Trigger Start and Wait for Ready..

Parameter 1							
Host Raw Memory Access Address bits 15-8							
15	14	13	12	11	10	9	8
Host Raw Memory Access Address bits 7-0							
7	6	5	4	3	2	1	0

Parameter 2							
Reserved						Host Raw Memory Access Address bits 25-24	
15	14	13	12	11	10	9	8
Host Raw Memory Access Address bits 23-16							
7	6	5	4	3	2	1	0

Parameter 3							
Host Raw Memory Access Count bits 15-8							
15	14	13	12	11	10	9	8
Host Raw Memory Access Count bits 7-0							
7	6	5	4	3	2	1	0

Parameter 4							
Reserved						Host Raw Memory Access Count bits 25-24	
15	14	13	12	11	10	9	8
Host Raw Memory Access Count bits 23-16							
7	6	5	4	3	2	1	0

For a detailed description of the bits in Parameters 1-4, see the REG[0144h] ~ REG[014Ah] register descriptions in A.3.5, “Host Interface Memory Access Configuration” on page 177.

9.6.19 BST_END_SDR (0x1E + 0 parameters)

This command terminates a burst operation before it has completed.

Note
Any memory operation in progress should be terminated with this command before a new memory operation is initiated.

Functions performed:
1. End Previous Host Memory access operation if currently active
2. Wait for Busy to end

9.6.20 LD_IMG (0x20 + 1 parameter)

This command starts a Full Frame Memory Load operation according to the data packing settings in parameter 1.

Functions performed:
1. End Previous Host Memory access operation if currently active.
2. Setup Write Mode and Packed Access Mode on REG[0140h]
3. Setup Packing Bpp Select using Parameter
4. Setup Full Display Size Update (Copy size from Display Engine's registers)
5. Trigger start transfer.

Parameter 1							
n/a							
15	14	13	12	11	10	9	8
n/a		Data Packing Select bits 1-0		n/a			
7	6	5	4	3	2	1	0

For a detailed description of the bits in Parameter 1, see the REG[0140h] bits 5-4 bit description in A.3.5, "Host Interface Memory Access Configuration" on page 177.

9.6.21 LD_IMG_AREA (0x22 + 5 parameters)

This command starts an Area Defined Frame Memory Load operation according to the data packing settings in the parameters.

Functions performed:
1. End Previous Host Memory access operation if currently active.
2. Setup Write Mode and Packed Access Mode on REG[0140h]
3. Setup Packing Bpp Select using Parameter
4. Setup Size with Parameters.
5. Trigger start transfer

Parameter 1

n/a							
15	14	13	12	11	10	9	8
n/a		Data Packing Select bits 1-0		n/a			
7	6	5	4	3	2	1	0

For a detailed description of the bits in Parameter 1, see the REG[0140h] bits 5-4 bit description in A.3.5, “Host Interface Memory Access Configuration” on page 177.

Parameter 2

n/a			Reserved	Packed Pixel Rectangular X-Start Position bits 11-8			
15	14	13	12	11	10	9	8
Packed Pixel Rectangular X-Start Position bits 7-0							
7	6	5	4	3	2	1	0

Parameter 3

n/a			Reserved	Packed Pixel Rectangular Y-Start Position bits 11-8			
15	14	13	12	11	10	9	8
Packed Pixel Rectangular Y-Start Position bits 7-0							
7	6	5	4	3	2	1	0

Parameter 4

n/a			Packed Pixel Rectangular Width bits 12-8				
15	14	13	12	11	10	9	8
Packed Pixel Rectangular Width bits 7-0							
7	6	5	4	3	2	1	0

Parameter 5

n/a			Packed Pixel Rectangular Height bits 12-8				
15	14	13	12	11	10	9	8
Packed Pixel Rectangular Height bits 7-0							
7	6	5	4	3	2	1	0

For a detailed description of the bits in Parameters 2-5, see the REG[014Ch] ~ REG[0152h] register descriptions in A.3.5, “Host Interface Memory Access Configuration” on page 177.

9.6.22 LD_IMG_END (0x23 + 0 parameters)

This command terminates a Load Image operation before it has completed and waits for the image load to finish before writing to the Memory.

Note
Any memory operation in progress should be terminated with this command before a new memory operation is initiated.

Functions performed:
1. End Previous Host Memory access operation if currently active.
2. Wait for Busy to end

9.6.23 LD_IMG_WAIT (0x24 + 0 parameters)

This command waits for a Load Image operation to finish writing to the memory.

Functions performed:
1. Wait for REG[0140h] bit 12 - wait for busy to deassert.

9.6.24 LD_IMG_SETADR (0x25 + 2 parameters)

This command sets the manual address where the host will load an image.

Functions performed:
1. Set REG[0140h] bit 7 to select destination start address defined by Host Raw Memory Access.
2. Set Host Raw Memory Access address using the parameters.

Parameter 1

Host Raw Memory Access Start Address bits 15-8							
15	14	13	12	11	10	9	8
Host Raw Memory Access Address bits 7-0							
7	6	5	4	3	2	1	0

Parameter 2

n/a						Host Raw Memory Access Address bits 25-24	
15	14	13	12	11	10	9	8
Host Raw Memory Access Address bits 23-16							
7	6	5	4	3	2	1	0

For a detailed description of the bits in Parameters 1-2, see the REG[0144h] ~ REG[0146h] register descriptions in A.3.5, “Host Interface Memory Access Configuration” on page 177.

9.6.25 LD_IMG_DSPEADR (0x26 + 0 parameters)

This command sets the address where the host will load an image to be the address specified by the Display Engine image buffer (see REG[0310h] ~ REG[0312h]).

Functions performed:
1. Clear REG[0140h] bit 7 to select destination start address defined by Display Engine image buffer start address.

9.6.26 WAIT_DSPE_TRG (0x28 + 0 parameters)

This command waits for the Display Engine operation to complete.

Functions performed:
1. Wait for REG[0338h] bit 0 to return 0b

9.6.27 WAIT_DSPE_FREND (0x29 + 0 parameters)

This command wait for the Display Engine to complete outputting display frames.

Functions performed:
1. Wait for REG[0338h] bit 3 to return 0b

9.6.28 WAIT_DSPE_LUTFREE (0x2A + 0 parameters)

This command wait for the Display Engine to have at least one free LUT.

Functions performed:
1. Wait for REG[0338h] bit 5 to return 1b

9.6.29 WAIT_DSPE_MLUTFREE (0x2B + 1 parameter)

This command waits for the Display Engine to have at least one free Masked LUT.

Functions performed:
1. Setup LUT Mask register with parameter 1 (must not be set to 0000h)
2. Wait for REG[0338h] bit 6 to return 1b

Parameter 1							
LUT Mask Setting 15-8							
15	14	13	12	11	10	9	8
LUT Mask Setting 7-0							
7	6	5	4	3	2	1	0

For a detailed description of the bits in Parameter 1, see the REG[032Eh] bit descriptions in A.3.16, “Display Engine: Component Control” on page 213.

9.6.30 RD_WFM_INFO (0x30 + 2 parameters)

This command issues a Waveform Read operation to the Display Engine.

Functions performed:
1. Setup Waveform Address
2. Trigger Waveform Read operation
3. Wait for Trigger completed

Parameter 1							
Waveform Header Serial Flash Address bits 15-8							
15	14	13	12	11	10	9	8
Waveform Header Serial Flash Address bits 7-0							
7	6	5	4	3	2	1	0

Parameter 2							
n/a							
15	14	13	12	11	10	9	8
Waveform Header Serial Flash Address bits 23-16							
7	6	5	4	3	2	1	0

For a detailed description of the bits in Parameters 1-2, see the REG[0350h] ~ REG[0352h] register descriptions in A.3.21, “Display Engine: Serial Flash Waveform Registers” on page 238.

9.6.31 UPD_INIT (0x32 + 0 parameters)

This command issues an Update Buffer Refresh with data from the Image Buffer. No display operation will occur.

9.6.32 UPD_FULL (0x33 + 1 parameter)

This command issues a Full Frame Full Update operation to the Display Engine.

Parameter 1							
n/a	Border Update Enable	n/a		Display Update Waveform Mode bits 3-0			
15	14	13	12	11	10	9	8
Display Update LUT Select bits 3-0				n/a			
7	6	5	4	3	2	1	0

For a detailed description of the bits in Parameter 1, see the REG[0334h] bit descriptions in A.3.17, “Display Engine: Control/Trigger Registers” on page 216.

9.6.33 UPD_FULL_AREA (0x34 + 5 parameters)

This command issues an Area Defined Full Update operation to the Display Engine.

Functions performed:
1. Setup Display Engine Area Search Dimension
2. Trigger Full Area update with Parameter 1.

Parameter 1							
n/a	Border Update Enable	n/a		Display Update Waveform Mode bits 3-0			
15	14	13	12	11	10	9	8
Display Update LUT Select bits 3-0				n/a			
7	6	5	4	3	2	1	0

For a detailed description of the bits in Parameter 1, see the REG[0334h] bit descriptions in A.3.17, “Display Engine: Control/Trigger Registers” on page 216.

Parameter 2							
n/a			Reserved	Area Update Pixel Rectangular X-Start Position bits 11-8			
15	14	13	12	11	10	9	8
Area Update Pixel Rectangular X-Start Position bits 7-0							
7	6	5	4	3	2	1	0

Parameter 3							
n/a			Reserved	Area Update Pixel Rectangular Y-Start Position bits 11-8			
15	14	13	12	11	10	9	8
Area Update Pixel Rectangular Y-Start Position bits 7-0							
7	6	5	4	3	2	1	0

Parameter 4							
n/a			Area Update Pixel Rectangular Width bits 12-8				
15	14	13	12	11	10	9	8
Area Update Pixel Rectangular Width bits 7-0							
7	6	5	4	3	2	1	0

Parameter 5							
n/a			Area Update Pixel Rectangular Height bits 12-8				
15	14	13	12	11	10	9	8
Area Update Pixel Rectangular Height bits 7-0							
7	6	5	4	3	2	1	0

For a detailed description of the bits in Parameter 2-5, see the REG[0340h] ~ REG[0346h] register descriptions in A.3.20, “Display Engine: Partial Update Configuration Register” on page 232.

9.6.34 UPD_PART (0x35 + 1 parameter)

This command issues a Partial Update operation to the Display Engine. This operation affects changed pixels only.

Functions performed:
1. Trigger Partial update with Parameter 1

Parameter 1							
n/a	Border Update Enable	n/a		Display Update Waveform Mode bits 3-0			
15	14	13	12	11	10	9	8
Display Update LUT Select bits 3-0				n/a			
7	6	5	4	3	2	1	0

For a detailed description of the bits in Parameter 1, see the REG[0334h] bit descriptions in A.3.17, “Display Engine: Control/Trigger Registers” on page 216.

9.6.35 UPD_PART_AREA (0x36 + 5 parameters)

This command issues an Area defined Partial Update operation to the Display Engine. This operation affects changed pixels only.

Functions performed:
1. Setup Display Engine Area Search Dimension
2. Trigger Full Area update with Parameter 1.

Parameter 1							
n/a	Border Update Enable	n/a		Display Update Waveform Mode bits 3-0			
15	14	13	12	11	10	9	8
Display Update LUT Select bits 3-0				n/a			
7	6	5	4	3	2	1	0

For a detailed description of the bits in Parameter 1, see the REG[0334h] bit descriptions in A.3.17, “Display Engine: Control/Trigger Registers” on page 216.

Parameter 2							
n/a			Reserved	Area Update Pixel Rectangular X-Start Position bits 11-8			
15	14	13	12	11	10	9	8
Area Update Pixel Rectangular X-Start Position bits 7-0							
7	6	5	4	3	2	1	0

Parameter 3							
n/a			Reserved	Area Update Pixel Rectangular Y-Start Position bits 11-8			
15	14	13	12	11	10	9	8
Area Update Pixel Rectangular Y-Start Position bits 7-0							
7	6	5	4	3	2	1	0

Parameter 4							
n/a			Area Update Pixel Rectangular Width bits 12-8				
15	14	13	12	11	10	9	8
Area Update Pixel Rectangular Width bits 7-0							
7	6	5	4	3	2	1	0

Parameter 5							
n/a			Area Update Pixel Rectangular Height bits 12-8				
15	14	13	12	11	10	9	8
Area Update Pixel Rectangular Height bits 7-0							
7	6	5	4	3	2	1	0

For a detailed description of the bits in Parameter 2-5, see the REG[0340h] ~ REG[0346h] register descriptions in A.3.20, “Display Engine: Partial Update Configuration Register” on page 232.

9.6.36 UPD_GDRV_CLR (0x37 + 0 parameters)

This command issues a display sequence output on the Gate Driver only. This command is used to clear the unknown state of the Gate Driver display at power-up.

9.6.37 UPD_SET_IMGADR (0x38 + 2 parameters)

This command sets the Display Engine Image Buffer Start Address.

Parameter 1							
Image Buffer Start Address bits 15-8							
15	14	13	12	11	10	9	8
Image Buffer Start Address bits 7-0							
7	6	5	4	3	2	1	0

Parameter 2							
n/a						Image Buffer Start Address bits 25-24	
15	14	13	12	11	10	9	8
Image Buffer Start Address bits 23-16							
7	6	5	4	3	2	1	0

For a detailed description of the bits in Parameters 1-2, see the REG[0310h] ~ REG[0312h] register descriptions in A.3.15, “Display Engine: Memory Region Configuration Registers” on page 212.

Chapter 10 Display Memory Configurations

10.1 Introduction

The S1D13521 controller manages its memory in 2 different areas.

- **Image Buffer Area**
  - Host can consider the Image Buffer as the display buffer area.
  - Image Buffer data is always stored in unpacked 1 byte per pixel format.
  - Appropriate bits from the byte are used for grey-scale conversion
    (Most Significant bit is always utilized).
  - Memory location is configurable (see REG[0310h] ~ REG[0312h]).
  - Memory size requirement for the Image Buffer area is:
    Roundup32(Display Width) x Display Height x 1 byte
- **Update Buffer Area**
  - Update Buffer is used for internal update operations only. It should be not accessed by the Host.
  - Update Buffer data requires 2 bytes per pixel.
  - Contains the current display pixel value which should match the state of the panel.
  - Memory location is configurable (see REG[0314h] ~ REG[0316h]).
  - Memory size requirement for the Update Buffer area is:
    Display Width x Display Height x 2 bytes

The recommended location for the Update Buffer in memory is address 0x00000000. Having the Update Buffer at this address allows Mobile SDRAM to partially self-refresh this area during standby and sleep mode. The following diagram shows an example configuration for the SDRAM.

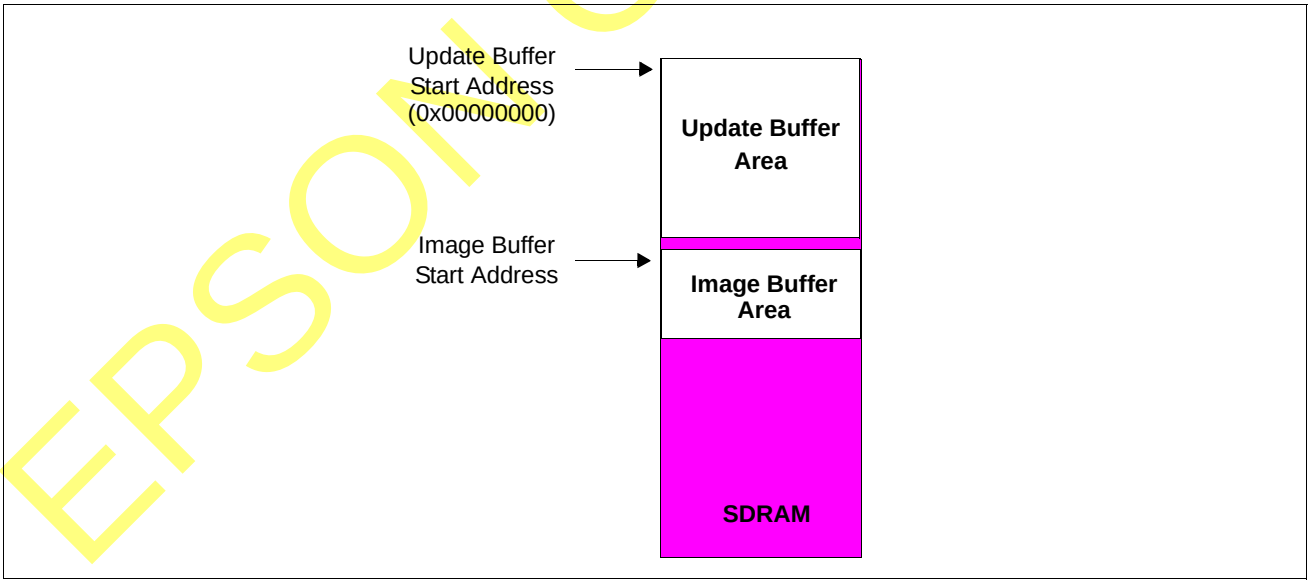


Figure 10-1: S1D13521 Memory Area Configuration Example

10.2 Image Buffer Memory Area Setup

The S1D13521 controller supports destructive partial region writes to the Image Buffer area. A predefined memory start region can be defined using the Host commands (see 9.5, “Command List” on page 58). The memory start region is referenced as the Image Buffer Start Address position in the memory.

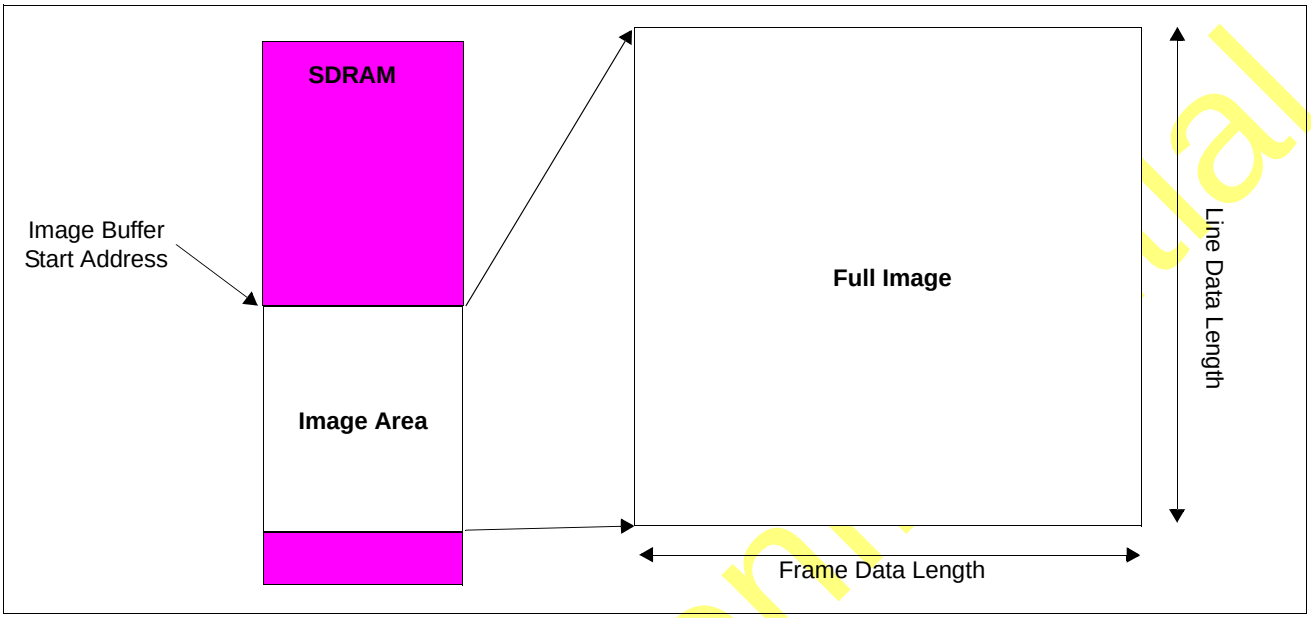


Figure 10-2: Full Image Area Setup

For any partial write using the predefined area (configured using the XStart, YStart, Width, and Height parameters), the S1D13521 automatically calculates the start memory address position.

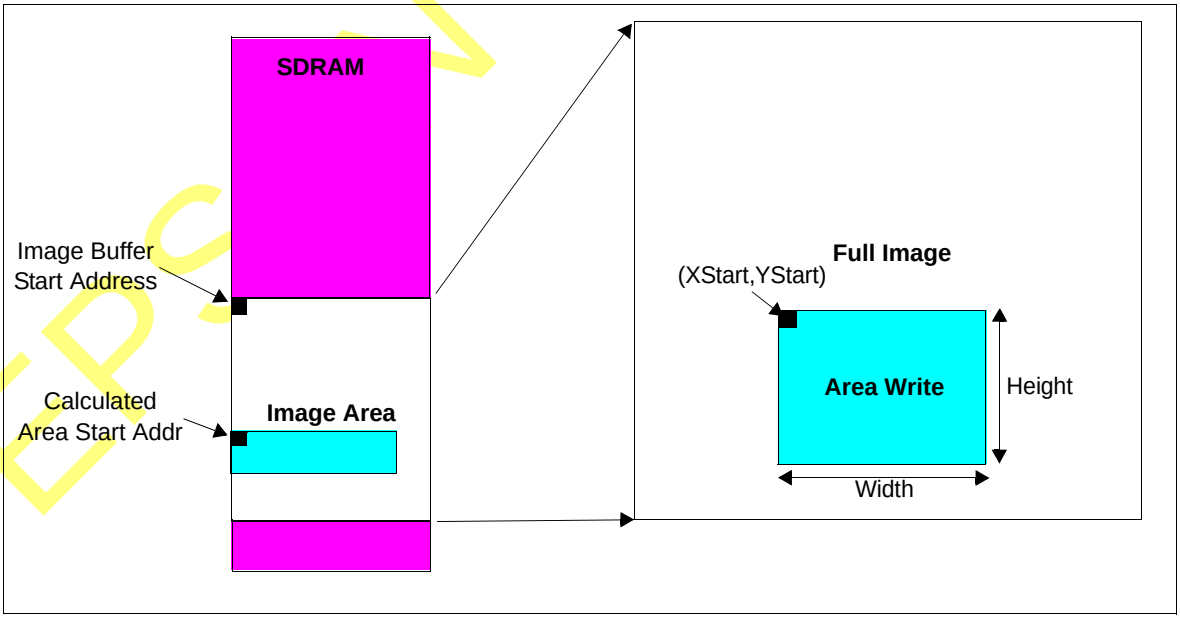


Figure 10-3: Host Memory Area Setup

10.2.1 Image Buffer Storage

Unprocessed pixel data is stored in the Image Buffer in raster sequence. The address pointer is defined by the Image Buffer Start Address bits, REG[0310h] ~ REG[0312h].

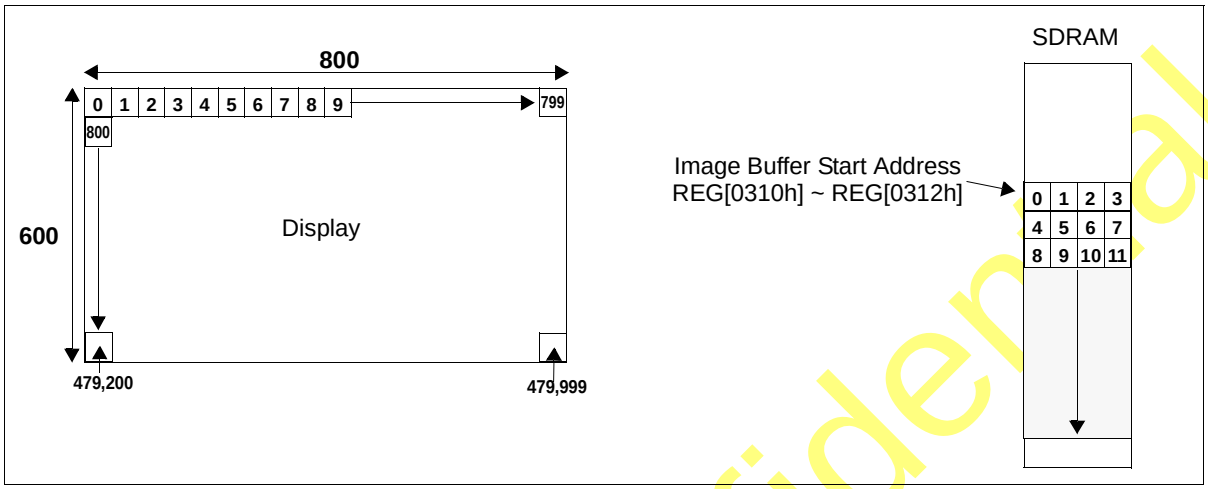


Figure 10-4: Image Buffer Storage Example - 800x600 Display Size

The Image Buffer horizontal size must be a multiple of 32. When the horizontal display size is not divisible by 32, additional “dummy” pixels are used to pad the display. For example, for a 1200x825 display size, the closest size divisible by 32 is 1216. The extra padded pixels are stored in the SDRAM.

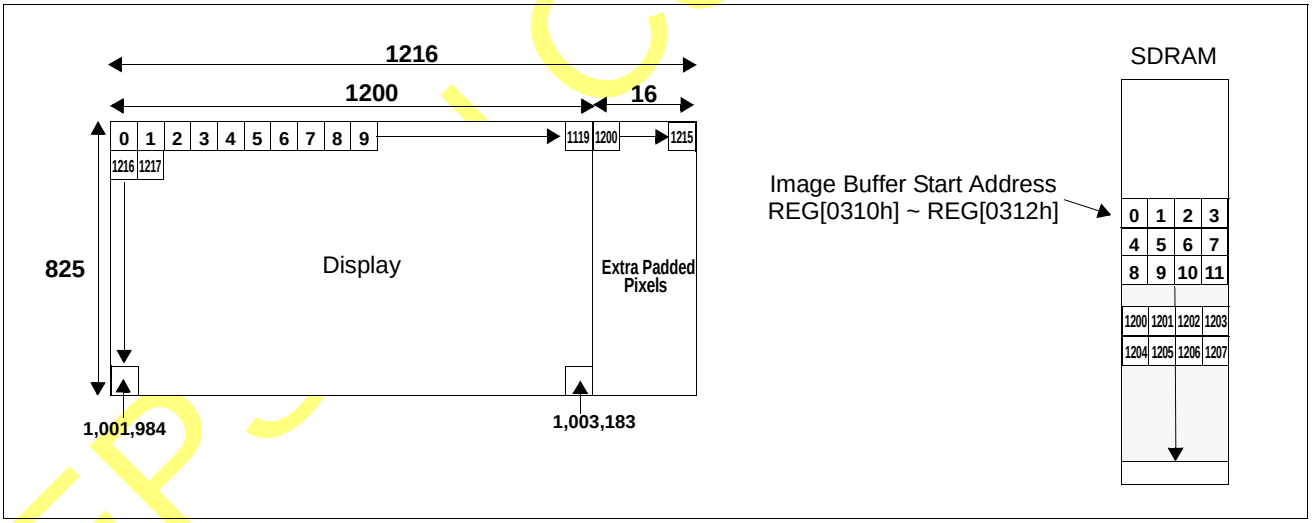


Figure 10-5: Image Buffer Storage Example - 1200x825 Display Size

Note

When Packed Pixel access mode is used (REG[0140h] bit 0 = 1b), the extra padded pixels do not have to be written to the image buffer (i.e. burst write a 1200x825 packed image into the image buffer).

When Raw Pixel access mode is used (REG[0140h] bit 0 = 0b), the extra padded pixels must be written to the image buffer (i.e. burst write a 1216x825, instead of 1200x825, 1 Byte-per-pixel image into the image buffer).

10.2.2 Multiple Image Buffer Support

Multiple Image Buffers may be useful for software applications when page caching or creating Pop-Up windows. The Host software can setup multiple image buffers through manual configuration using the following commands.

- Image Buffer Start Address using the UPD_SET_IMGADR command.
- Host packed mode Write Start address by using the LD_IMG_SETADR command.

The following figure shows a multiple Image Buffer configuration.

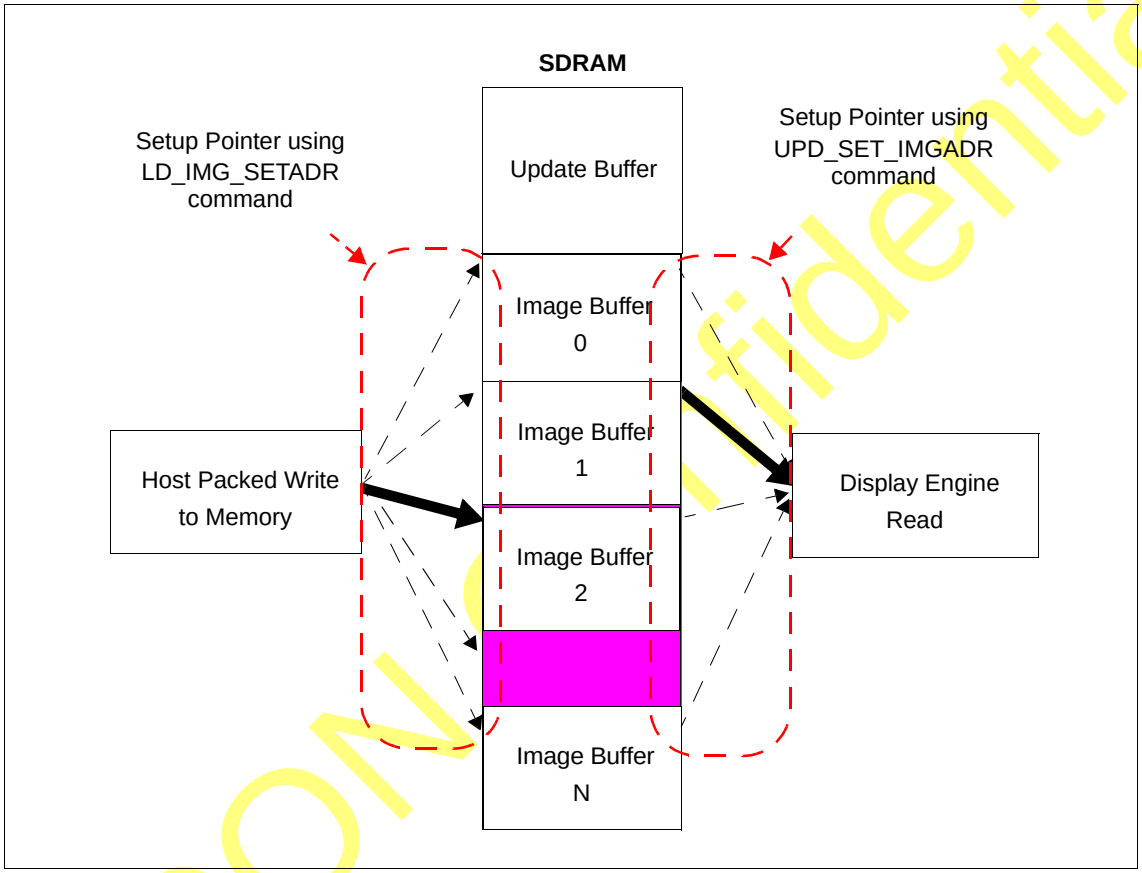


Figure 10-6: Multiple Image Buffer Configuration

10.3 Update Buffer Memory Area Setup

The S1D13521 requires that the Update Buffer memory area is located such that it does not overlap with the Image Buffer memory area. The Update Buffer start address is configured using REG[0314h] and REG[0316h]. The recommended location for the Update Buffer in memory is address 0x00000000. Having the Update Buffer at this address allows Mobile SDRAM to perform a Partial-Bank Refresh operation and retain the Update Buffer contents with minimal power consumption.

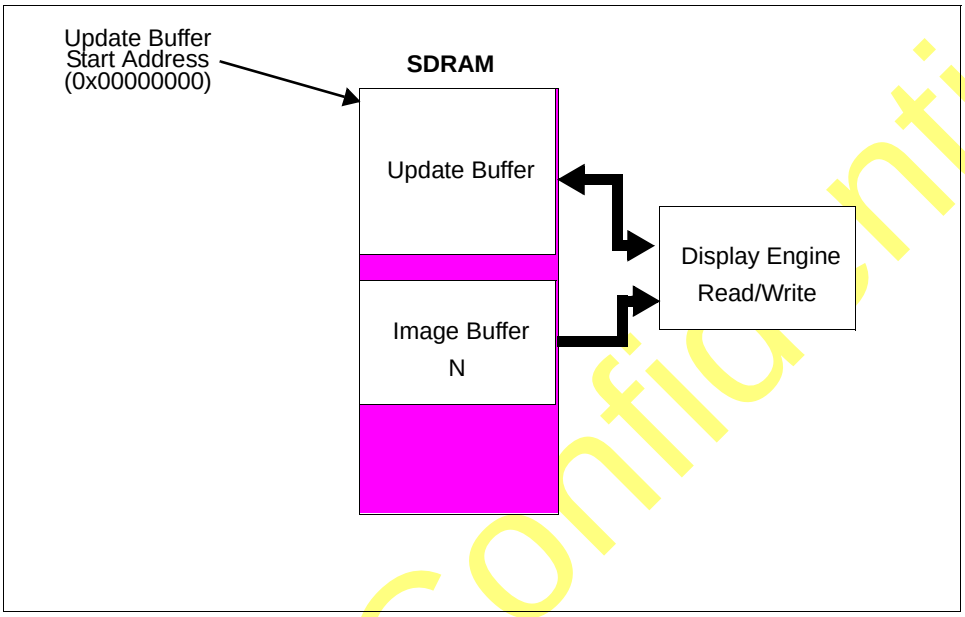


Figure 10-7: Update Buffer Memory Start Address Setup

10.3.1 Update Buffer Usage

The Update Buffer contains the current pixel value/state of the EPD panel. It is recommended to perform initialization of the Update Buffer using the following commands:

- **UPD_INIT -** A software application should copy the last known pixel value of the panel to the Image Buffer and perform an UPD_INIT command which will synchronize the contents of the Update Buffer with the panel's pixel value.
- **UPD_FULL -** With waveform INIT (Waveform number 0), which will initialize the display panel to a known state. This should be used when the previous image cannot be retrieved for restoration.

The following programming flow shows how to initialize the Update Buffer and synchronize it with the display contents.

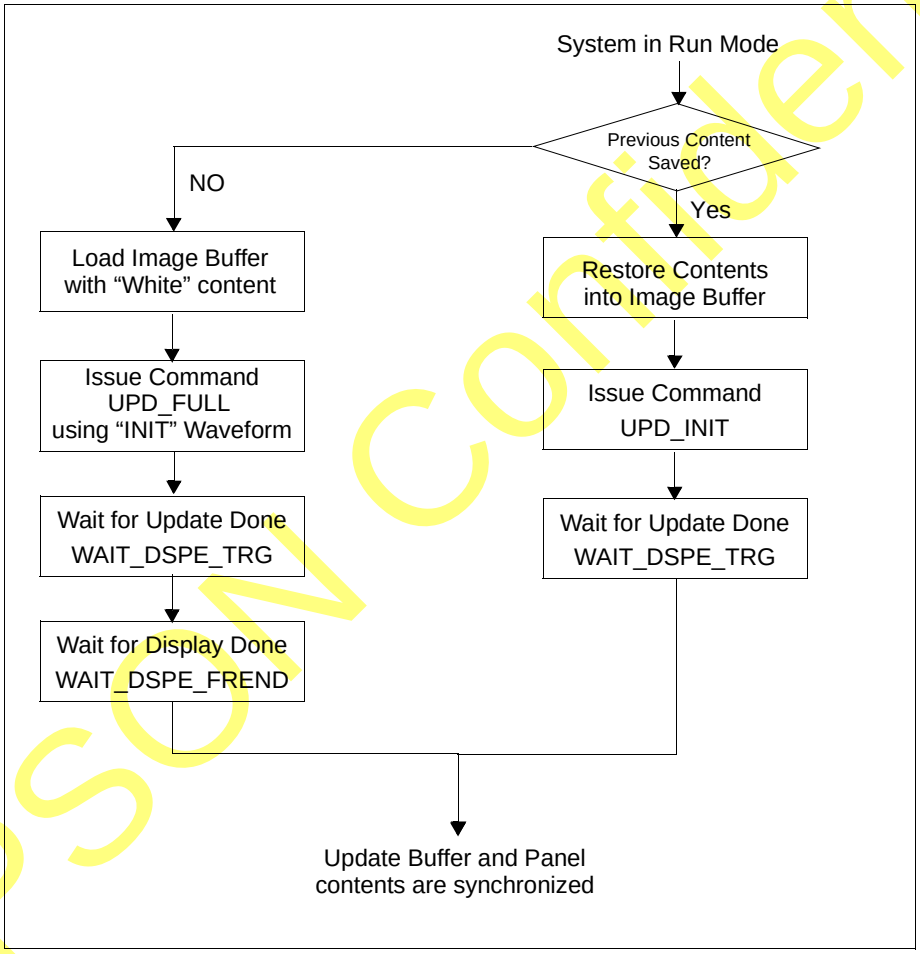


Figure 10-8: Update Buffer Initialization Programming Flow

10.4 Display Engine Usage of the Image Buffer

The S1D13521 stores every pixel in unpacked 1 byte format. For details on the Host unpacking procedure, refer to Chapter 11, “Host Memory Transfer Format” on page 94. The number of bits used depends on the configuration of the LUT Index Format Select bits, REG[0330h] bits 2-0. Only the appropriate Most-Significant-Bit(s) are used.

The following diagram shows which bits will be processed by the display engine.

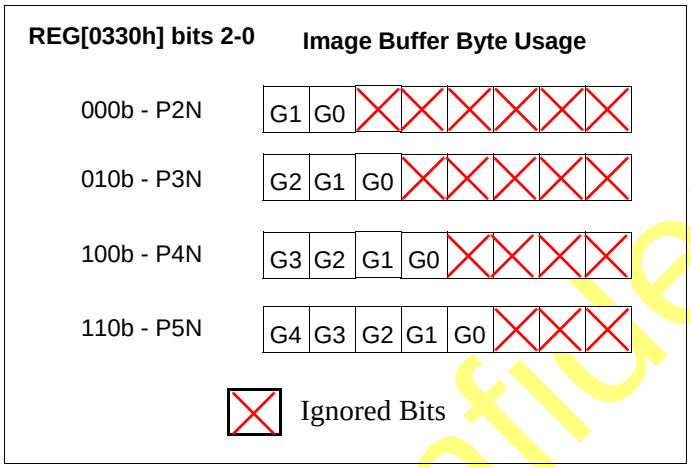


Figure 10-9: Image Buffer Bit Usage

10.5 Rotation Support

10.5.1 Rotation Introduction

Display panels are typically oriented in Landscape mode, where the Horizontal Size is larger than the Vertical Size. In this case, the display refresh occurs from Left to right and top to bottom.

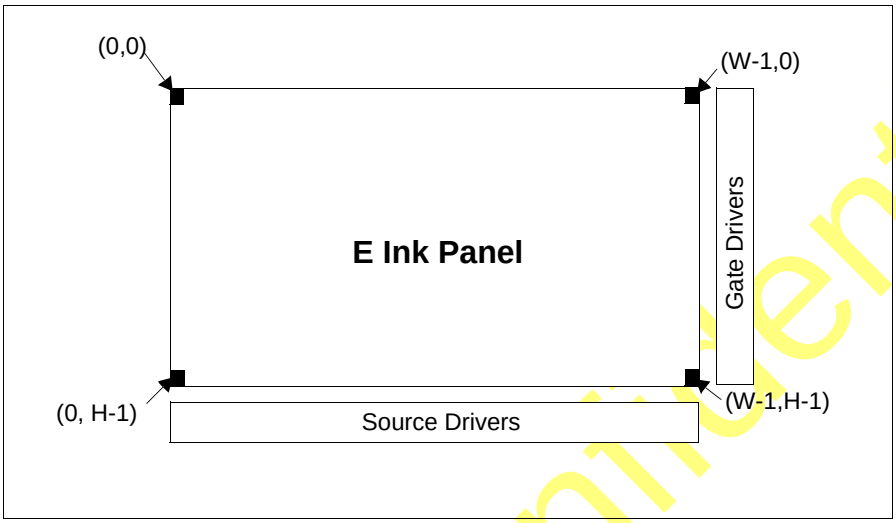


Figure 10-10: Landscape (0 Degrees) Display

The S1D13521 supports rotation modes that allow 90°, 180°, and 270° rotation in a counter-clockwise direction. The rotation is done in hardware and is transparent to the user for all display buffer writes.

The actual address translation is performed during the Host Write and the image data is stored in memory in the rotated orientation.

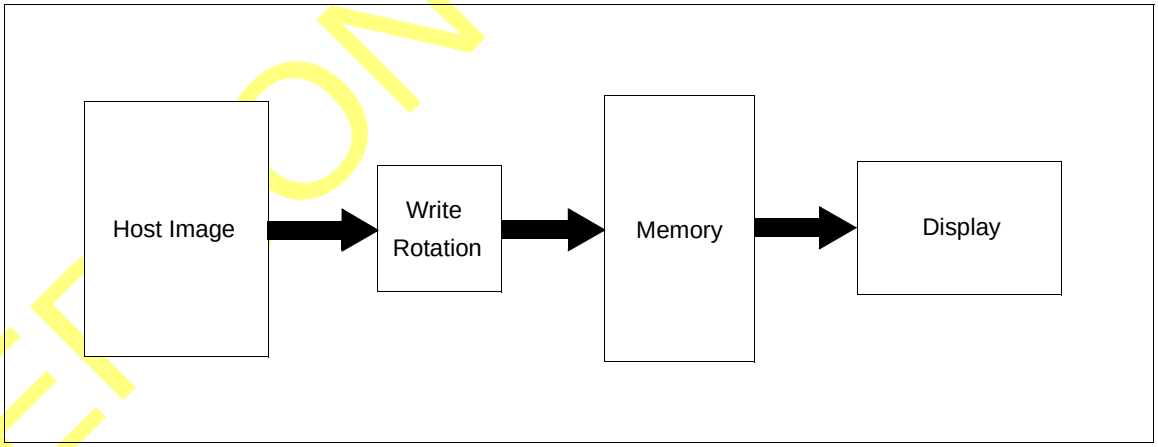


Figure 10-11: Write Rotation Flow in Hardware

Note
Memory Readback data does not support reverse-rotation.

10.5.2 90° Rotation

The following figure shows how the programmer sees a 600x800 portrait image and how the image is being displayed. The application image is written to the S1D13521 in the following sense: A–B–C–D. The display is refreshed in the following sense: B-D-A-C.

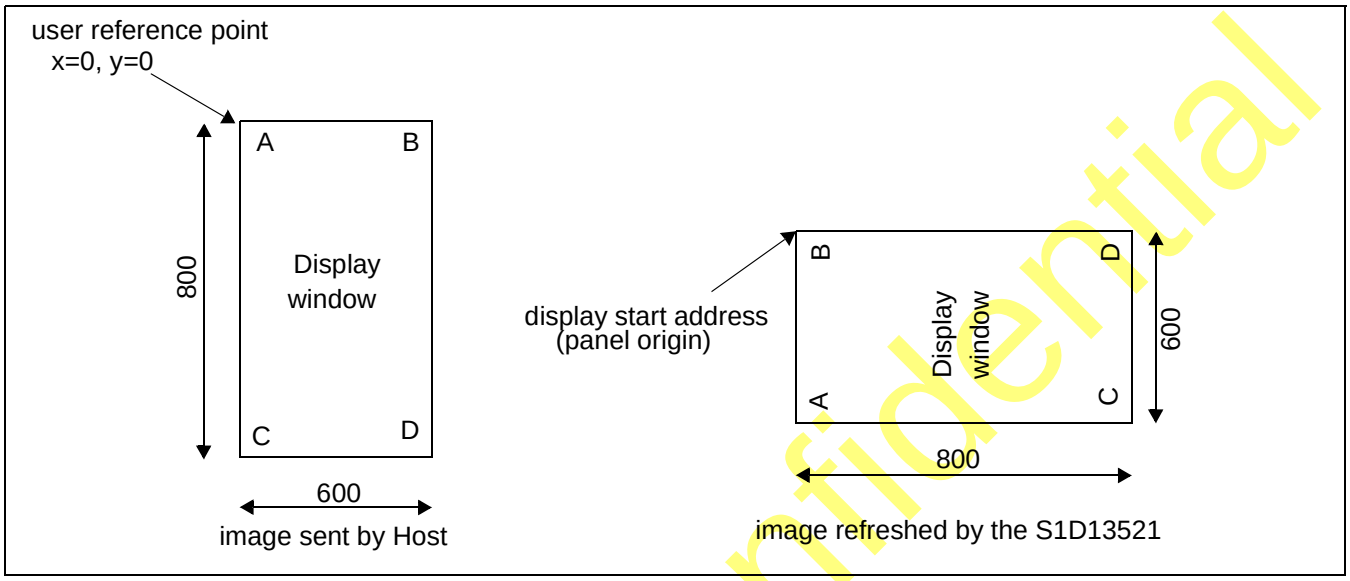


Figure 10-12: Relationship Between the Screen Image and the Image Refreshed in 90° Rotation

Programming

There are no special programming requirements other than enabling the rotation (see REG[0140h] bits 9-8). The start address and line offset are automatically calculated by the hardware.

10.5.3 180° Rotation

The following figure shows how the programmer sees a 800x600 landscape image and how the image is being displayed. The application image is written to the S1D13521 in the following sense: A–B–C–D. The display is refreshed in the following sense: D-C-B-A.

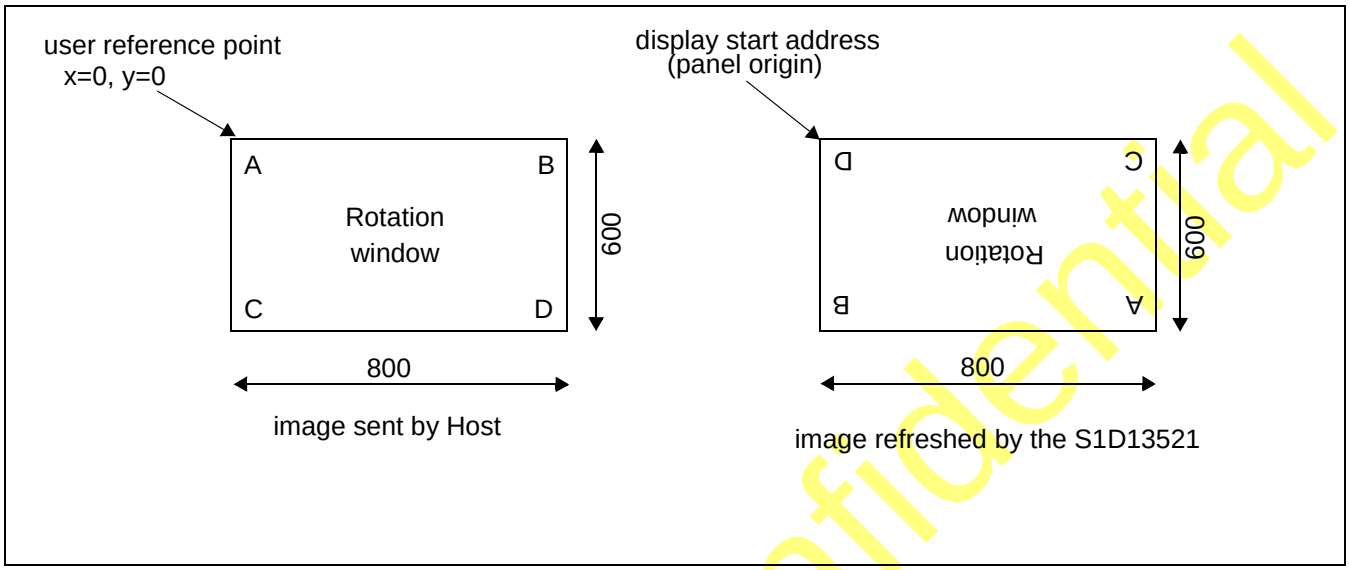


Figure 10-13: Relationship Between the Screen Image and the Image Refreshed in 180° Rotation

Programming

There are no special programming requirements other than enabling the rotation (see REG[0140h] bits 9-8). The start address and line offset are automatically calculated by the hardware.

10.5.4 270° Rotation

The following figure shows how the programmer sees a 600x800 portrait image and how the image is being displayed. The application image is written to the S1D13521 in the following sense: A–B–C–D. The display is refreshed in the following sense: C-A-D-B.

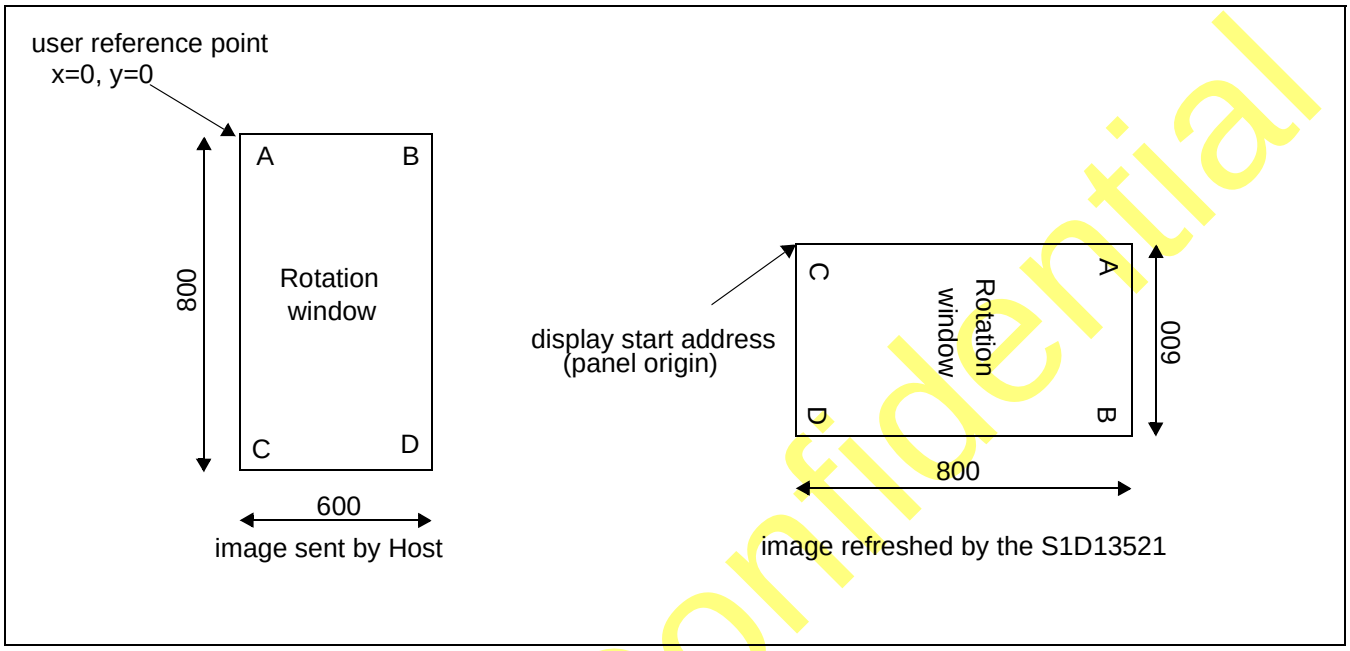


Figure 10-14: Relationship Between the Screen Image and the Image Refreshed in 270° Rotation

Programming

There are no special programming requirements other than enabling the rotation (see REG[0140h] bits 9-8). The start address and line offset are automatically calculated by the hardware.

10.6 Window Area Position / Rotation

For a Windowed Area write operation when rotation is enabled, the X-Start, Y-Start, Width and Height settings must be specified relative to **the user's own reference point**.

10.6.1 90° Rotation

The following figure shows how the Windowed Area is rotated on the displayed image. The application Window Area is written to the S1D13521 in the following sense: a–b–c–d.

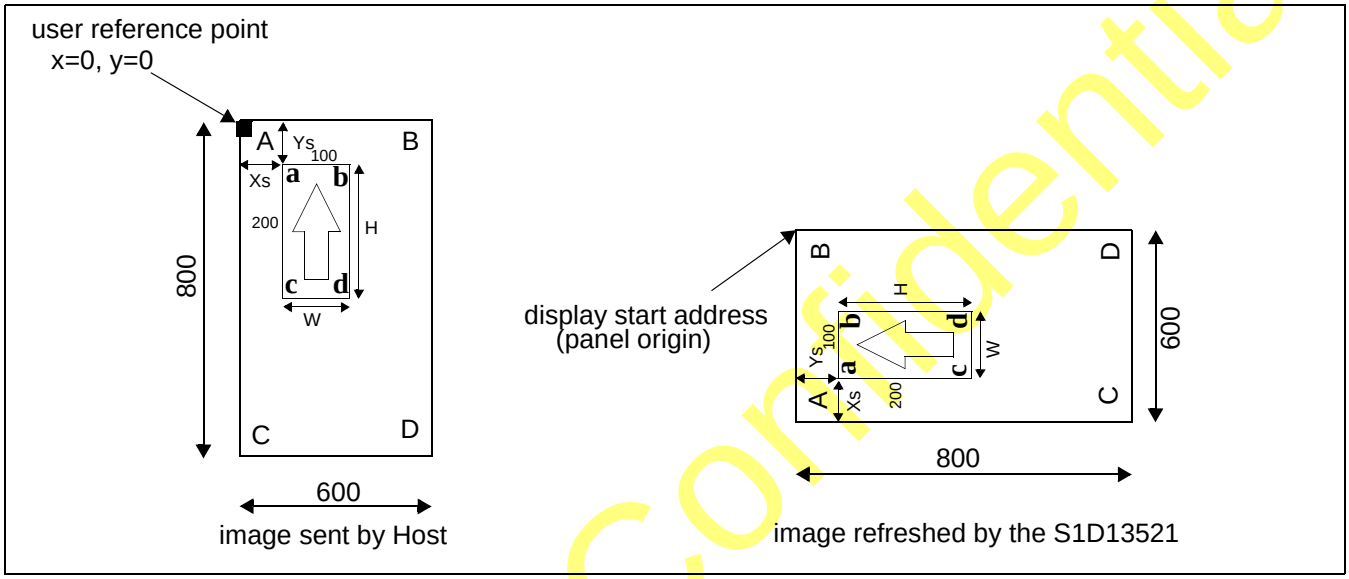


Figure 10-15: Relationship Between the Screen Window Area and the Image Refreshed in 90° Rotation

Programming

There are no special programming requirements other than enabling the rotation (see REG[0140h] bits 9-8). The start address and line offset are automatically calculated by the hardware.

10.6.2 180° Rotation

The following figure shows how the Windowed Area is rotated on the displayed image. The application Window Area is written to the S1D13521 in the following sense: a–b–c–d.

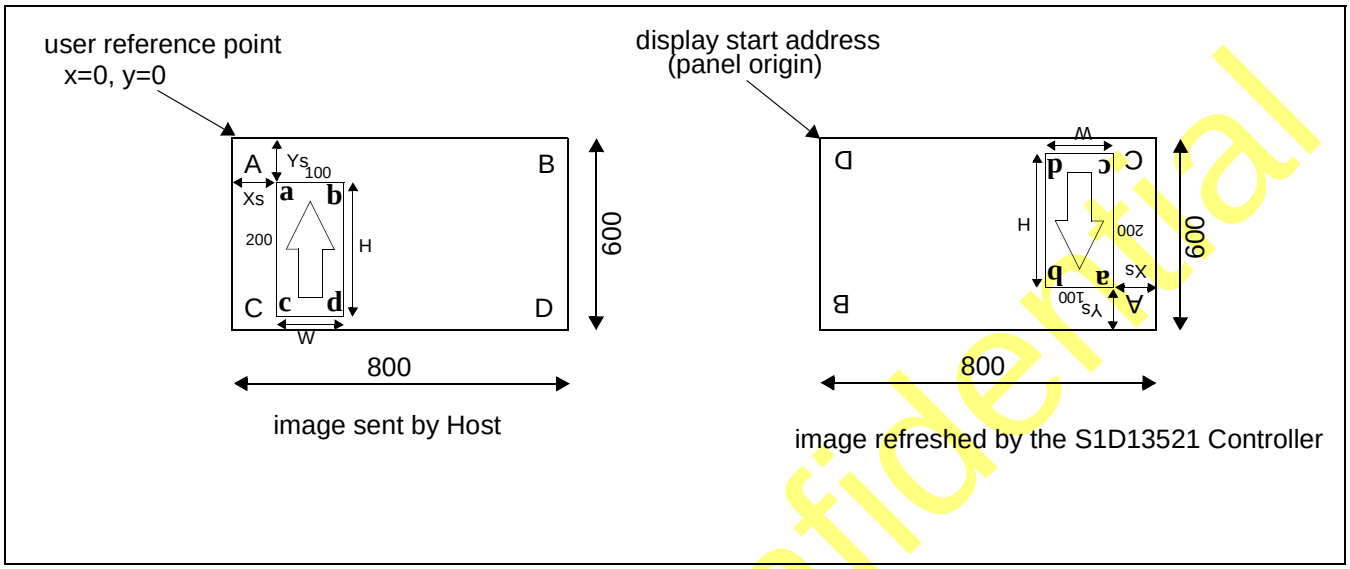


Figure 10-16: Relationship Between the Screen Window Area and the Image Refreshed in 180° Rotation

Programming

There are no special programming requirements other than enabling the rotation (see REG[0140h] bits 9-8). The start address and line offset are automatically calculated by the hardware.

10.6.3 270° Rotation

The following figure shows how the Windowed Area is rotated on the displayed image. The application Window Area is written to the S1D13521 in the following sense: a–b–c–d.

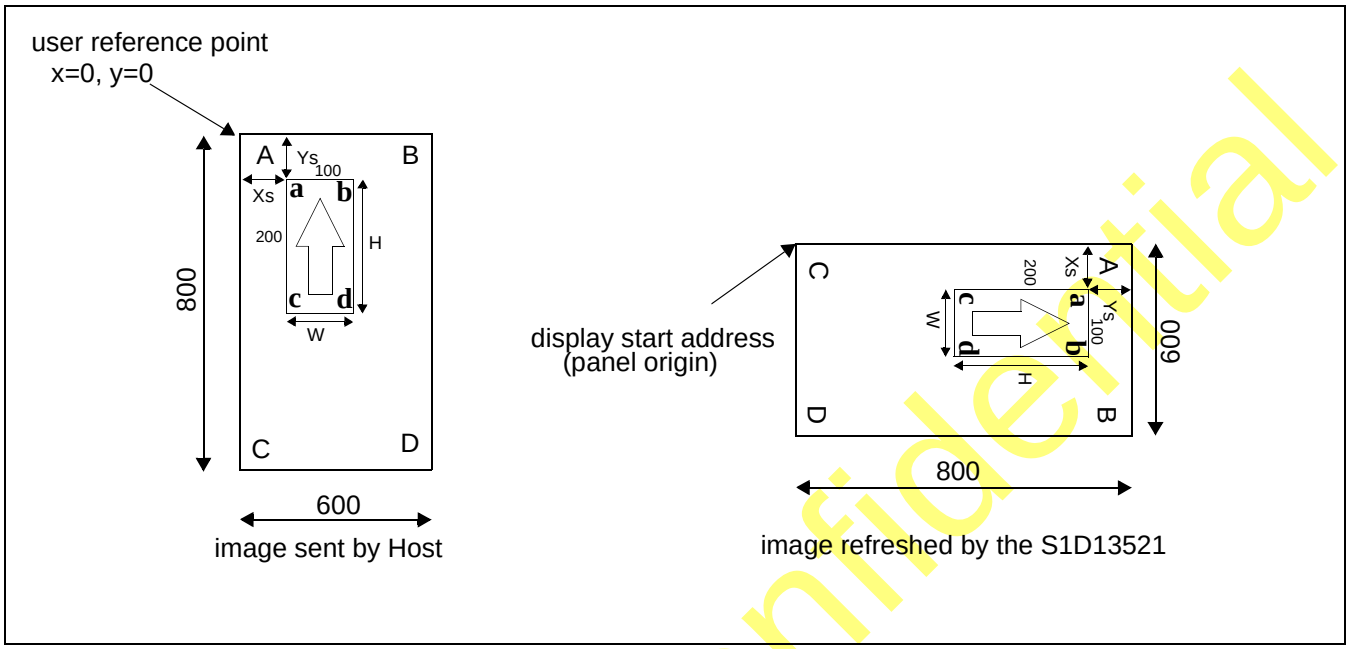


Figure 10-17: Relationship Between the Screen Window Area and the Image Refreshed in 270° Rotation

Programming

There are no special programming requirements other than enabling the rotation (see REG[0140h] bits 9-8). The start address and line offset are automatically calculated by the hardware.

10.7 Resolution Support

The S1D13521 supports resolutions of up to 4096 x 4096 pixels. However, resolutions greater than 2048 x 1536 cannot directly support a 50Hz frame rate and will require special considerations.

Also, for resolutions where the horizontal or the vertical resolution exceeds 2048 pixels, 0° and 180° rotation mode are not supported for host packed pixel mode.

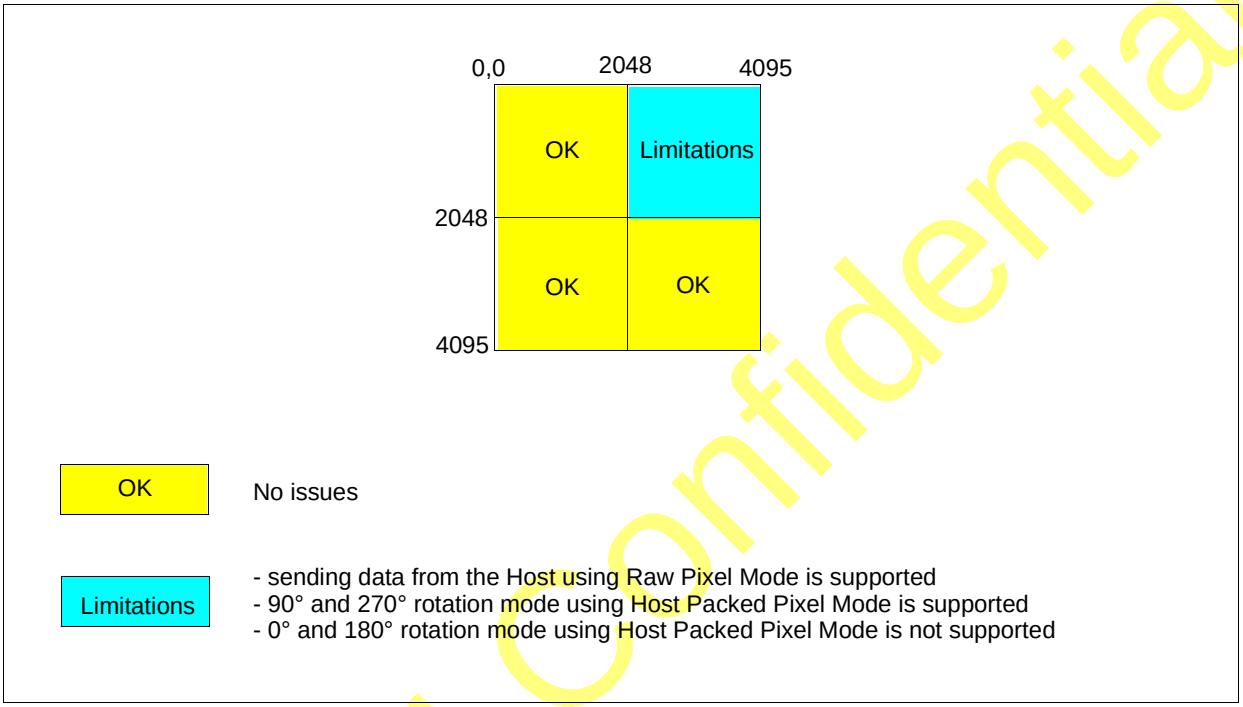


Figure 10-18: S1D13521 Resolutions

Chapter 11 Host Memory Transfer Format

11.1 Host Interface Memory Transfer Mode

Data transfers from the Host interface to memory can be performed using either packed pixel mode or raw memory mode. It is recommended that image data is only programmed into the Image Buffer memory area. The Image Buffer start address is configured using REG[0310h] ~ REG[0312h]. For further information on configuring the display memory, see Chapter 10, “Display Memory Configurations” on page 79.

Packed pixel mode “packs” multiple pixels into each data byte and provides a more efficient means of transferring pixel data to memory. Data transfers using raw memory mode always require one byte for each pixel. Raw memory mode also allows memory reads. Note that pixel packing is done only for the data transfer and pixel data is stored in memory using unpacked 1 byte format.

When the packed pixel data is unpacked, it is stored in the Image Buffer as shown below.

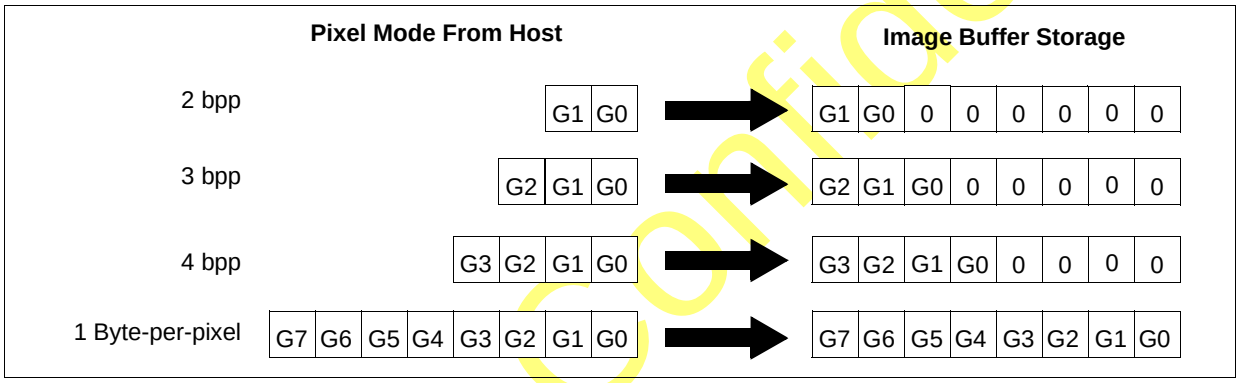


Figure 11-1: Packed Pixel Mode Data Unpacking Summary

The following figure provides a detailed description of the method used to unpack data and stored it in memory.

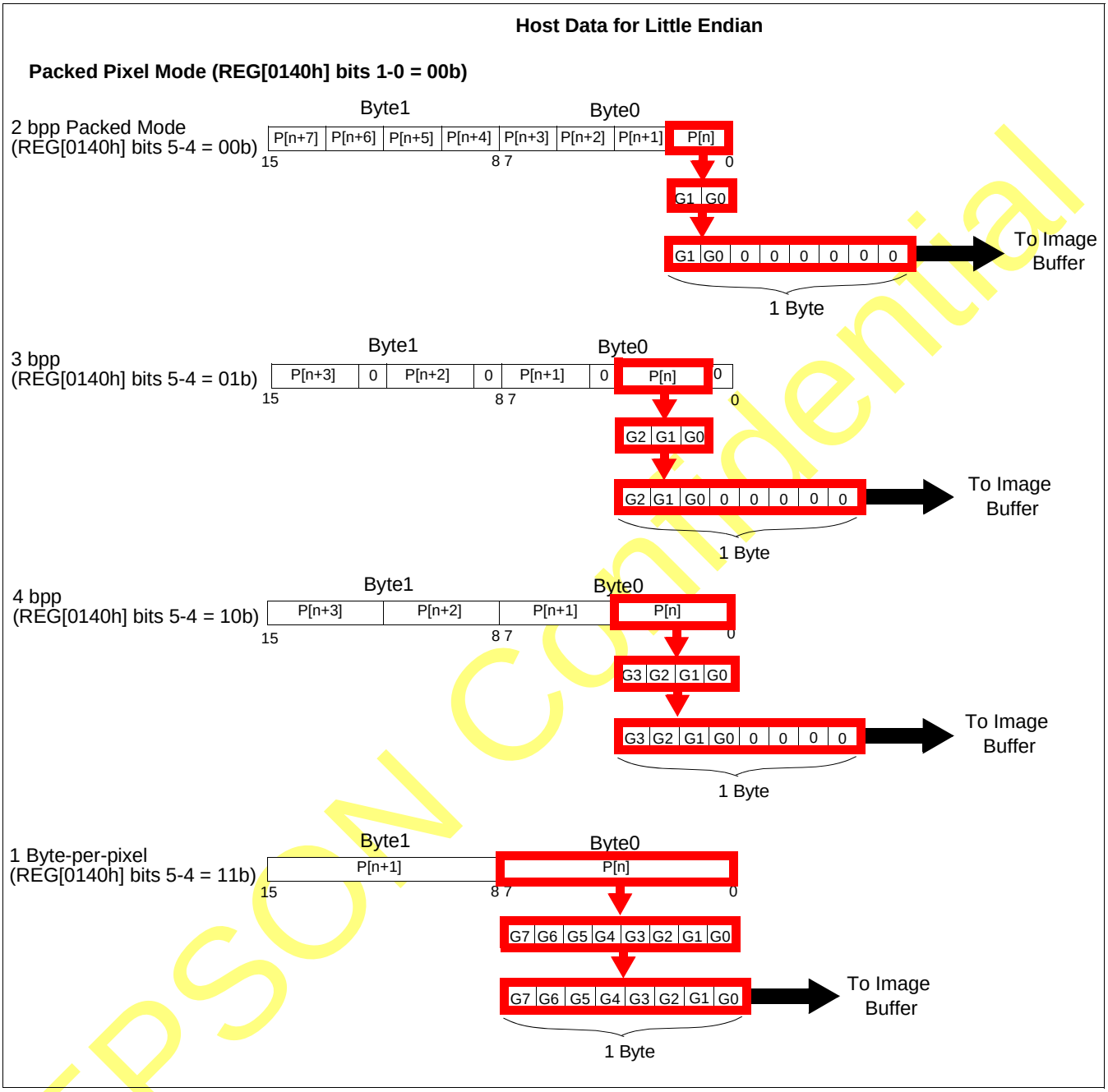


Figure 11-2: Packed Pixel Mode Data Unpacking Detailed Description

11.1.1 Display Engine LUT Format and Host Interface Packed Pixel Mode Compatibility

It is important to set the Host interface packed pixel data transfer mode to a setting that is compatible with Display Engine LUT format setting in REG[0330h] bits 2-0. For details on LUT format usage, refer to 10.4, “Display Engine Usage of the Image Buffer” on page 85.

The following table summarizes the compatible modes and settings.

Table 11-1: Display Engine LUT Format Compatibility with Host Packed Mode

Display Engine LUT Format Setting (REG[0330h] bits 2-0)	Host Interface Packed 2 bpp	Host Interface Packed 3 bpp	Host Interface Packed 4 bpp	Host Interface Packed 1 Byte-per-pixel
000b (P2N)	Yes	Yes	Yes	Yes
010b (P3N)	No	Yes	Yes	Yes
100b (P4N)	No	No	Yes	Yes
110b (P5N)	No	No	No	Yes

11.2 Host Interface Packed Pixel Data Transfer Format Endian Formatting

Memory accesses support both Little Endian and Big Endian data transfers (see REG[0020h] bit 1). The following figure shows the data transfer formats for Little Endian, REG[0020h] bit 1 = 0b.

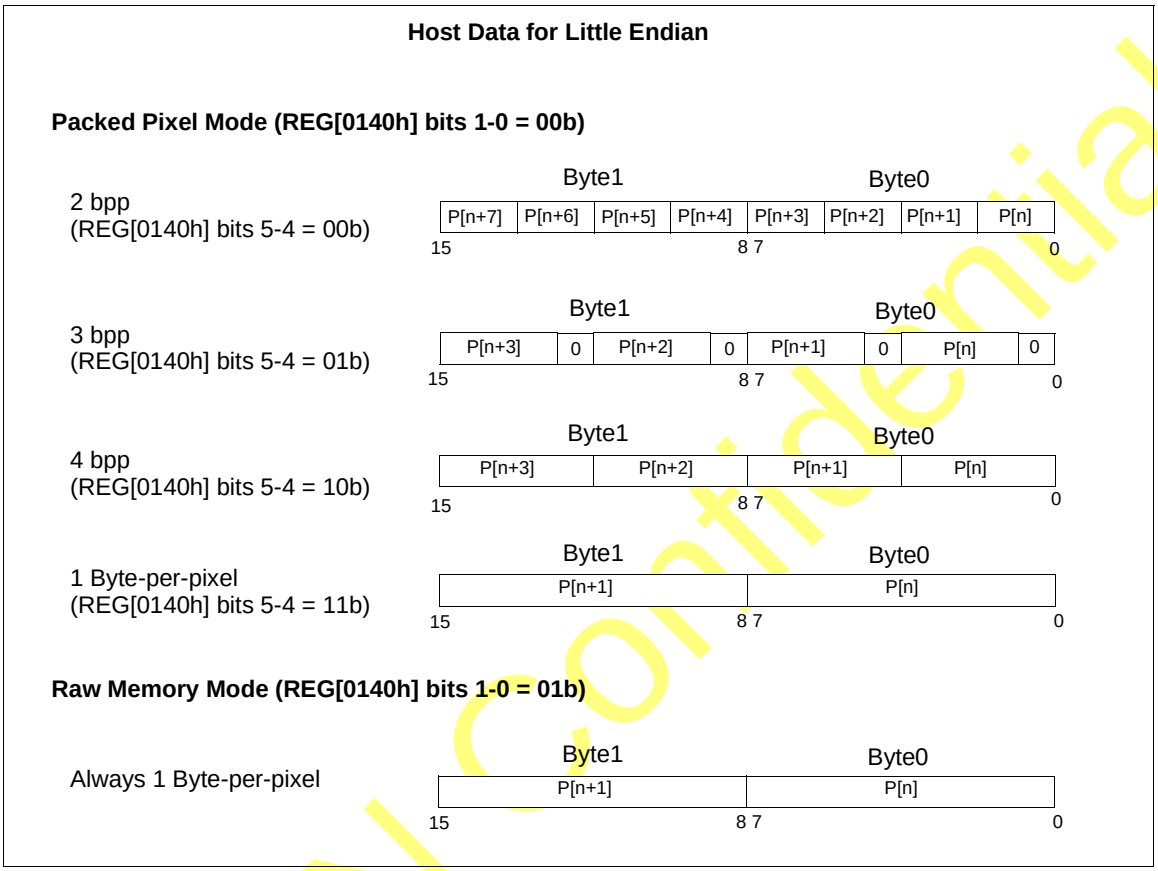


Figure 11-3: Host Interface Pixel Data Transfer Format for Little Endian

Note
For details on memory storage, see 10.2.1, “Image Buffer Storage” on page 81.

The following figure shows the data transfer formats for Big Endian, REG[0020h] bit 1 = 1b.

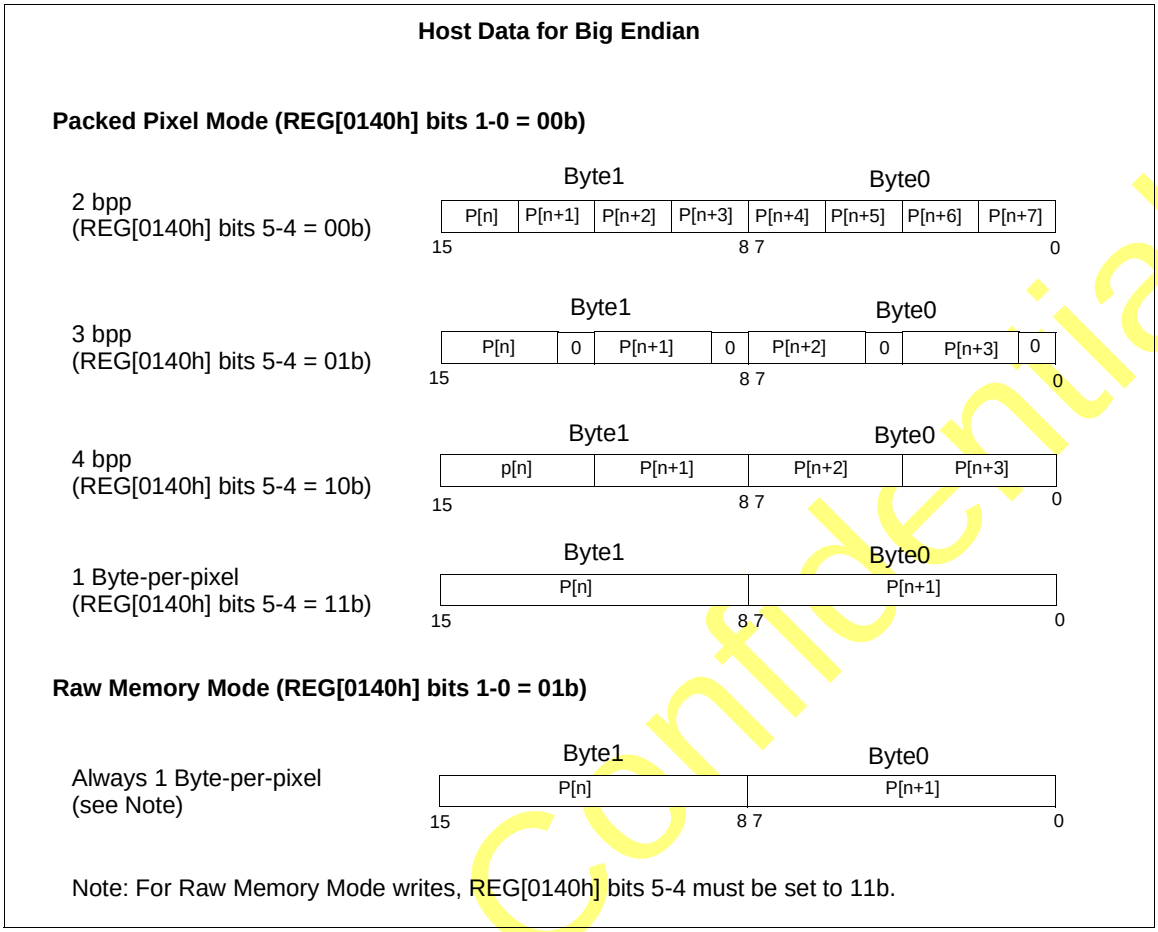


Figure 11-4: Host Interface Pixel Data Transfers Format for Big Endian

Note
For details on memory storage, see 10.2.1, “Image Buffer Storage” on page 81.

11.2.1 Packed Pixel Handling of Odd Display Widths for 90/270° Rotation

When using a landscape panel size of 1200x825, for 90° and 270° rotations packed image writes will be 825x1200 and any odd pixels within each line will be not be written to the Image Buffer Memory when using following the scheme below:

Number of dummy pixels in each line = (Number of Pixels Packed Per 16-bit Write - (Rotated Width Pixel Size%Number of Pixels Packed Per 16-bit Write))

The following example is using 90° Host Write Rotation for 825x1200 (rotated from 1200x825) single line Write.

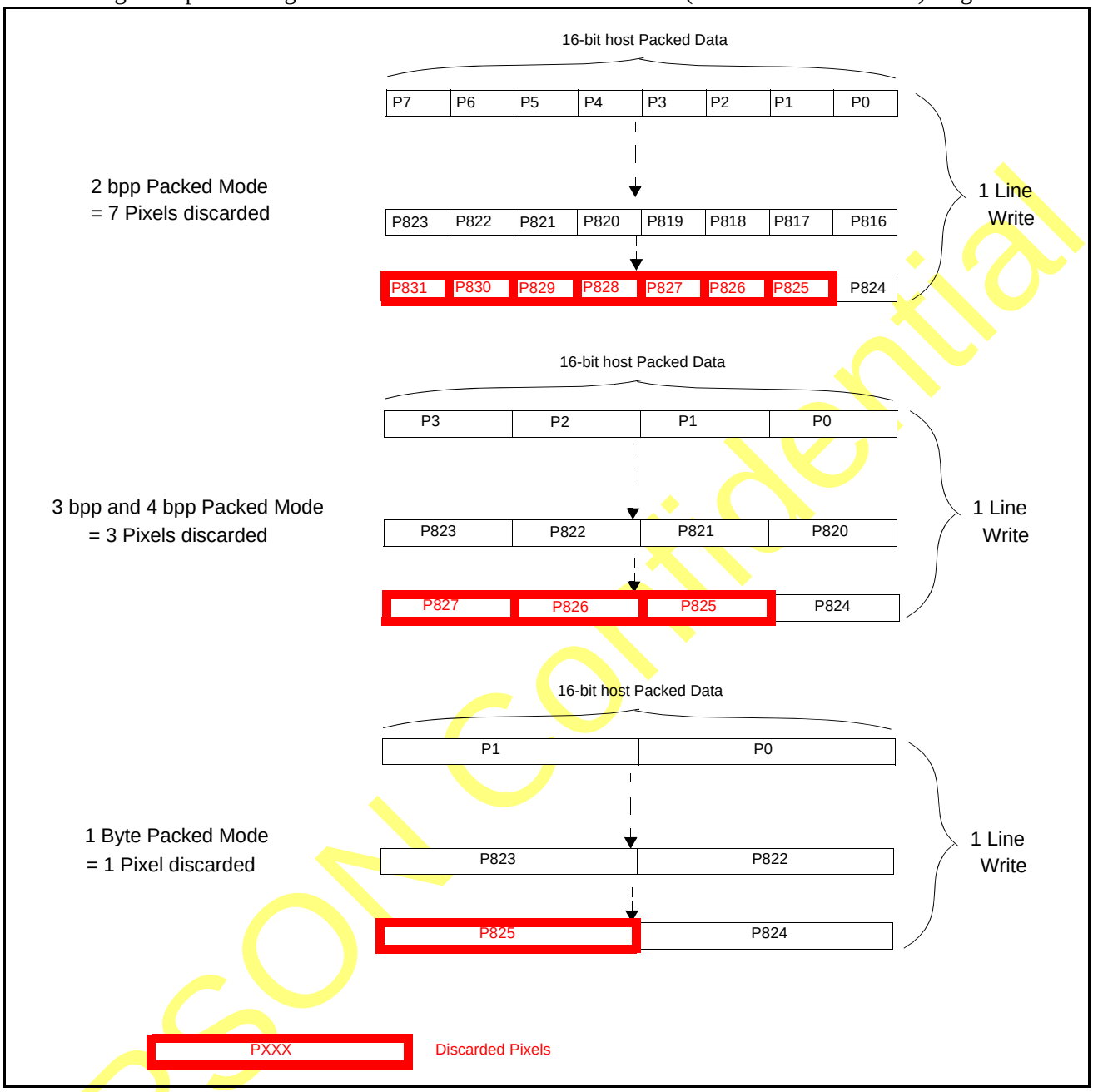


Figure 11-5: Example of Packed Pixels Odd Display Width Size Write

Note

This only applies to edge of the panel when in 90 degrees and 180 degrees Rotation. For area based writes, refer to 11.2.2, “Packed Pixel Area Size Transfer Limitations” on page 100

11.2.2 Packed Pixel Area Size Transfer Limitations

The packed pixel format requires certain limitations to be observed for all host image data transfers. The following size limitations must be observed for each bpp mode.

Table 11-2: Host Interface Pixel Data Transfer Limitations

Bpp Mode	Width limitation	Height limitation
2 bpp	Must be multiple of 8 pixels	Minimum of 1 Line
3 bpp	Must be multiple of 4 pixels	Minimum of 1 Line
4 bpp	Must be multiple of 4 pixels	Minimum of 1 Line
5 bpp or 1 Byte-per-pixel	Must be multiple of 2 pixels	Minimum of 1 Line

Chapter 12 Display Operations

12.1 Display Update: Multi-Region LUT Pipeline Usage

The S1D13521 Display Engine includes a high-performance 16-Region LUT pipeline. Each pipeline region may be assigned to:

- A group of pixels which do not overlap another pipeline region operation. The group of pixels doesn't need to be an enclosed rectangular region.
- A temperature compensated waveform Update Mode.

12.1.1 User Interface Applications with Multi-Region LUT Pipeline

The 16-Region LUT Pipeline is designed to provide fast response for User Interface applications while still maintaining the waveform update requirements and speed limitations. The 16-Region LUT Pipeline is ideal for updating menu buttons, scroll bars, cursors, pen drawing, etc.

The following example shows a typical use for the 16-Region LUT Pipeline.

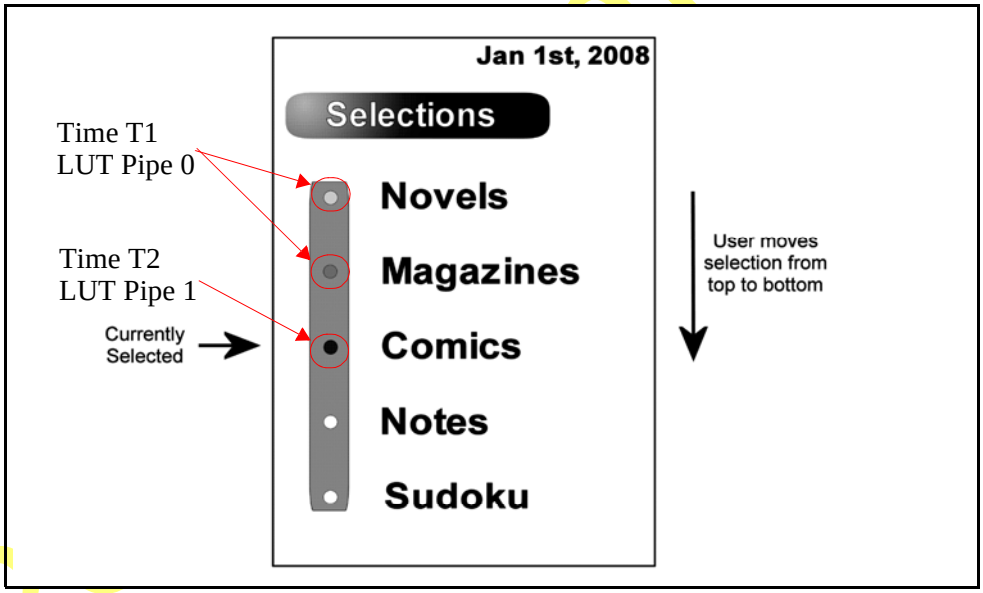


Figure 12-1: Example of a Simple Menu Button Movement

In the example, the starting position of the menu button is Novels. When the user moves the button from Novels to Magazines (T1), LUT pipeline 0 may be initiated to update the 2 buttons to the desired state. However, this update may take up to 260ms to be completed. If the user further moves the button to Comics within the 260ms update time (T2), LUT pipeline 1 may be assigned to the new position without waiting for the LUT pipeline 0 to complete its assigned update operation.

The following figure shows the transition timing for the three buttons.

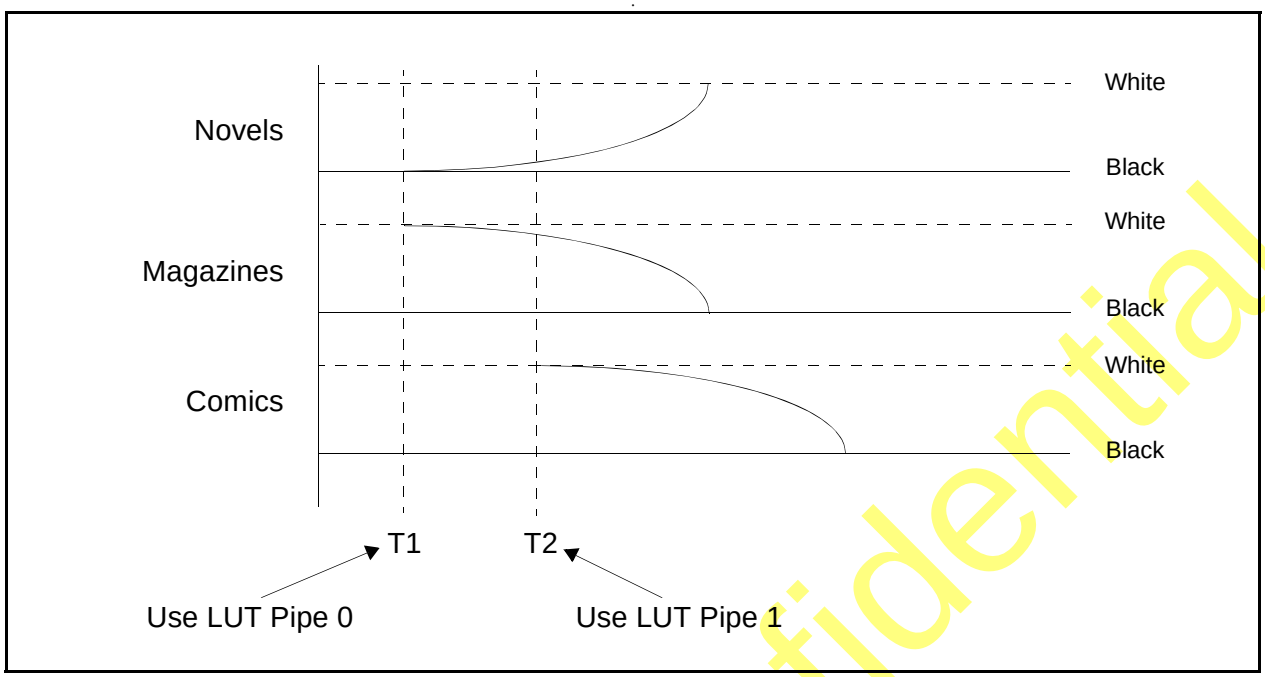


Figure 12-2: Transition Timing

12.1.2 Display Update Commands

There are four display update commands that may be used depending on the application requirement.

- UPD_FULL:
  This command forces an update on the entire display, even if the pixels have not changed levels.
- UPD_FULL_AREA
  This command forces an update on the defined rectangular area, even if the pixels have not changed levels.
- UPD_PART
  This command detects pixel changes between the image buffer and the current display for the entire display. Then, it updates the pixels with changed levels. If no pixel changes are detected, no display update takes place.
- UPD_PART_AREA
  This command detects pixel changes between the image buffer and the current display for the defined rectangular area. Then, it updates the pixels with changed levels. If no pixel changes are detected, no display update takes place.

12.1.3 Managing LUT Pipeline Usage

Manually Managing the LUT Pipeline

The Host software may manage the LUT pipeline manually by assigning a LUT pipeline number when using any of the UPD_FULL, UPD_FULL_AREA, UPD_PART or UPD_PART_AREA commands. The LUT pipeline number is specified in the Parameter 1 bits 7-4 (Display Update LUT select bits). When manually choosing the LUT pipeline, it is important not to select a busy LUT pipeline. The availability of the LUT pipeline can be checked using REG[0338h]. If a busy LUT is selected, the command will stop and report an error in the LUT Request Error Interrupt Raw Status bit, REG[033Ah] bit 9.

Automatic LUT Assignment

Optionally, the LUT pipeline may be managed by the S1D13521 (REG[0330h] bit 7 = 1b). When LUT auto select mode is enabled, the S1D13521 will automatically assign the highest numbered free LUT pipeline on any update display operation. If no LUT pipeline is available, the command will stop and report an error in the LUT Request Error Interrupt Raw Status bit, REG[033Ah] bit 9.

12.2 Guaranteed Display Update Operation Flow

Performing a display update operation involves 3 steps. In order to guarantee that the display update finishes completely, it is recommended that the Host software does not perform any image buffer memory write operations during Update Buffer Synthesis (step 2). Otherwise, the display may be only partially updated resulting in display "tearing".

1. **Host Memory Write Operation**
   The Host Memory Write Operation is dependent on the host software. For example, the Host may perform a multiple burst write before issuing an Update Trigger command.

2. **Update Buffer Synthesis**
   Once an Update Trigger command is issued, Update Buffer Synthesis is started. This step processes the data in the Image Buffer and places the appropriate data in the Update Buffer for the next display operation. The Update Buffer is not directly accessed by the Host software.

   Update Buffer Synthesis processing time is dependent on whether Display Frame Output is already active. If Display Frame Output is not currently active, Update Buffer Synthesis takes a maximum of 6ms for a 800x600 panel. If Display Frame Output is active, it takes a maximum of 2÷FrameRate for a 800x600 panel.

3. **Display Frame Output**
   Display Frame Output starts automatically right after Update Buffer Synthesis completes.

The following figure shows the Guaranteed Display Update Operation Flow steps.

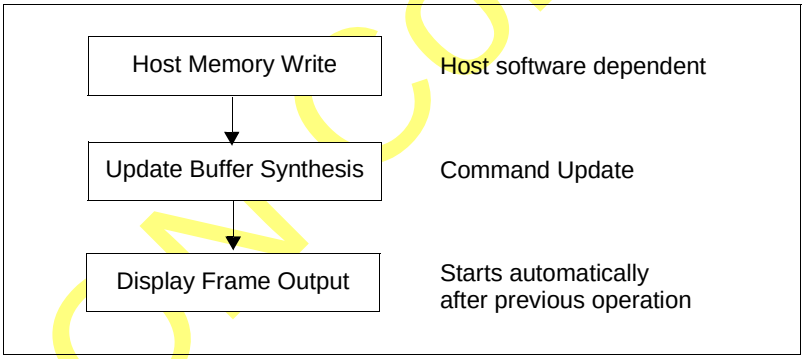


Figure 12-3: Guaranteed Display Update Operation Flow

12.3 Guaranteed Host Memory Write Display Trigger Operation Timing

When the Host software follows the guaranteed display update operation flow, the display timing below must be followed.

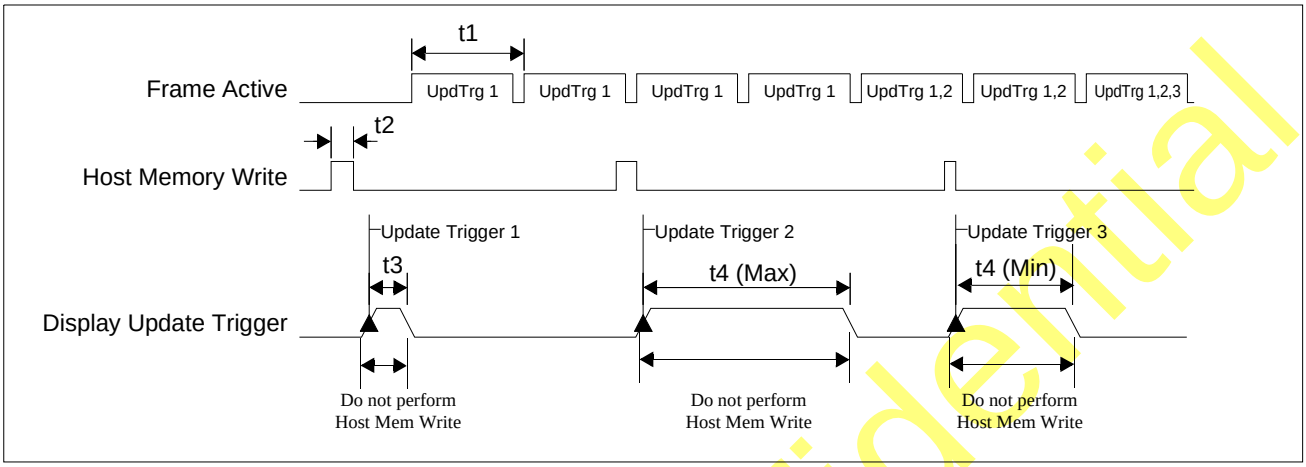


Figure 12-4: Guaranteed Display Update Timing

Table 12-1: Guaranteed Display Update Timing

Symbol	Parameter	Min	Max	Unit	Typical for 800x600x50hz
t1	Frame Period	1 ÷ FrameRate	1 ÷ FrameRate	s	20ms
t2	Host Memory Write Period	—	—	—	—
t3	Update Buffer Synthesis time when Frame is inactive	Note 1	Note 2	ns	Min: 2.3ms Max: 5ms
t4	Update Buffer Synthesis time when Frame is Active	t1 x 1	t1 x 2	s	Min: 20ms Max: 40ms

1. t3min = HSize x VSize x 2.5 ÷ 8 x 1 ÷ SYSCLK
2. t3max = HSize x VSize x 5.5 ÷ 8 x 1 ÷ SYSCLK

12.3.1 Guaranteed Display Update Operation Analysis

When the Guaranteed Display Update Operation flow is used, the operation starts with a Host memory write operation. Once the host memory write operation is complete, the Host software must trigger Update Buffer Synthesis to start. Since the Frame Update is not active, the Update Buffer Synthesis operation will be shorter. During this time, no image buffer memory writes should be performed by the Host.

The second Host memory write and update trigger operation occurs right after a frame. In this case, Update Buffer Synthesis takes the most processing time when the display is active. It takes up to 2 frames for Update Buffer Synthesis to process the requested Update Trigger. During this time, no image buffer memory write should be performed by the Host.

The third host memory write and update trigger operation occurs at the end of a frame. In this case, Update Buffer Synthesis the least processing time when the display is active (processing time is still shorter when the display is not active. It takes a minimum of 1 frame for Update Buffer Synthesis to process the requested Update Trigger. During this time, no image buffer memory write should be performed by the Host.

12.4 Asynchronous Host Memory Write Display Trigger Operation Timing

When guaranteed frame updates are not required (i.e. tearing is allowed), asynchronous display updates by the Host can be used for high performance operation. In this case, additional image buffer memory writes are performed during the Update Buffer Synthesis step.

When the Host software performs Asynchronous Display Updates, the display timing below must be followed.

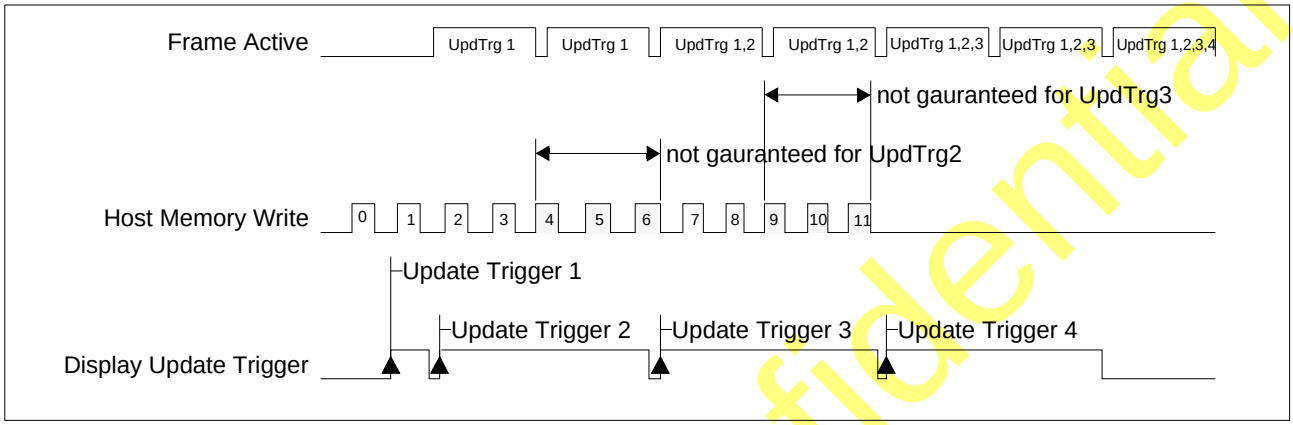


Figure 12-5: Asynchronous Display Update Timing

Table 12-2: Host Memory Write Effective Update

Update Trigger	Guaranteed Host Memory Write which will be updated fully	Not Guaranteed Host Memory Write which may be partially updated
1	0	1
2	0, 1, 2, 3	4, 5, 6
3	0, 1, 2, 3, 4, 5, 6, 7, 8	9, 10, 11
4	0, 1, 2, 3, 4, 5, 6, 7, 8, 9, 10, 11	NA

12.4.1 Asynchronous Display Update Operation Analysis

When Asynchronous Display Update Operations are performed, the operation starts with a Host memory write 0 operation. Once the host memory write operation is complete, the Host software must trigger Update Buffer Synthesis to start. Since the Frame Update is not active, the Update Buffer Synthesis operation will be shorter. During this time, Host memory write 1 is performed. Host memory write 1 data may be only partially displayed or not displayed at all.

Update Trigger 2 occurs right after the Update Trigger 1 process has completed. During Update Buffer Synthesis 2, the Host performs additional writes of block 2, 3, 4, 5, and 6. Only block data 2 and 3 will be guaranteed to be updated fully as Update Buffer synthesis only starts processing on the next available full frame.

Right after Update Buffer Synthesis 3, it is recommended to perform another Update Trigger (4) to ensure all non- guaranteed host write updates are reflected on the display.

12.5 Overlapping Display Update Operation Flow

12.5.1 Overlapping Display Updates

Under special conditions, an overlapping display update may be performed. An overlapping display update is defined as a partial display update that “overlaps” a display area which is already being updated. The following figure shows an example of this situation.

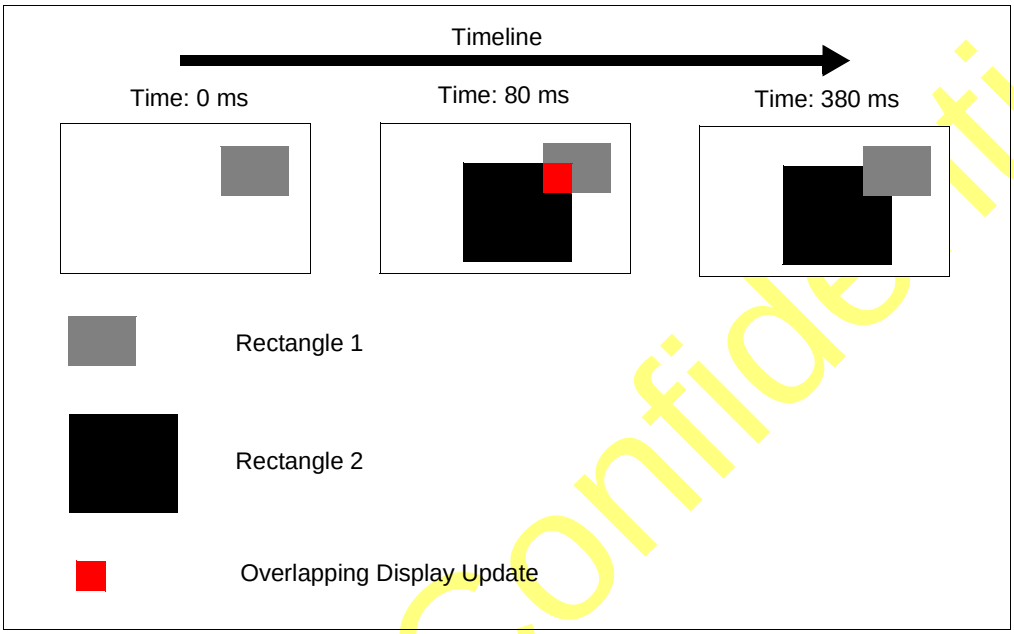


Figure 12-6: Overlapping Display Update Example

In this example, assume each display update will take 300 ms to complete. At time “0 ms”, the partial display update of Rectangle 1 is initiated. At time “80 ms”, a partial display update of Rectangle 2 is initiated. The area shown in “Red” is desired to have Rectangle 2 overlapping Rectangle 1. However, at time “380 ms”, once the partial display update of both rectangles are completed, rectangle 1 overlaps rectangle 2. To achieve the desired overlapping, the procedure described in 12.5.2, “Overlapping Display Update Recommended Programming Flow” on page 109 must be followed.

12.5.2 Overlapping Display Update Recommended Programming Flow

When overlapping display updates are performed, the LUT Area Overlap Conflict Interrupt Status and Raw Status bits (REG[033Ah] bit 7 and REG[033Ch] bit 7) can be used to detect Overlapping Display Update error conditions. This interrupt is triggered for every overlapping pixel, so it is recommended to check this bit only after the Image Buffer has been fully synthesized into the Update Buffer (after REG[0338h] bit 0 = 0b).

The following figure shows the recommended procedure to correct overlapping display update errors.

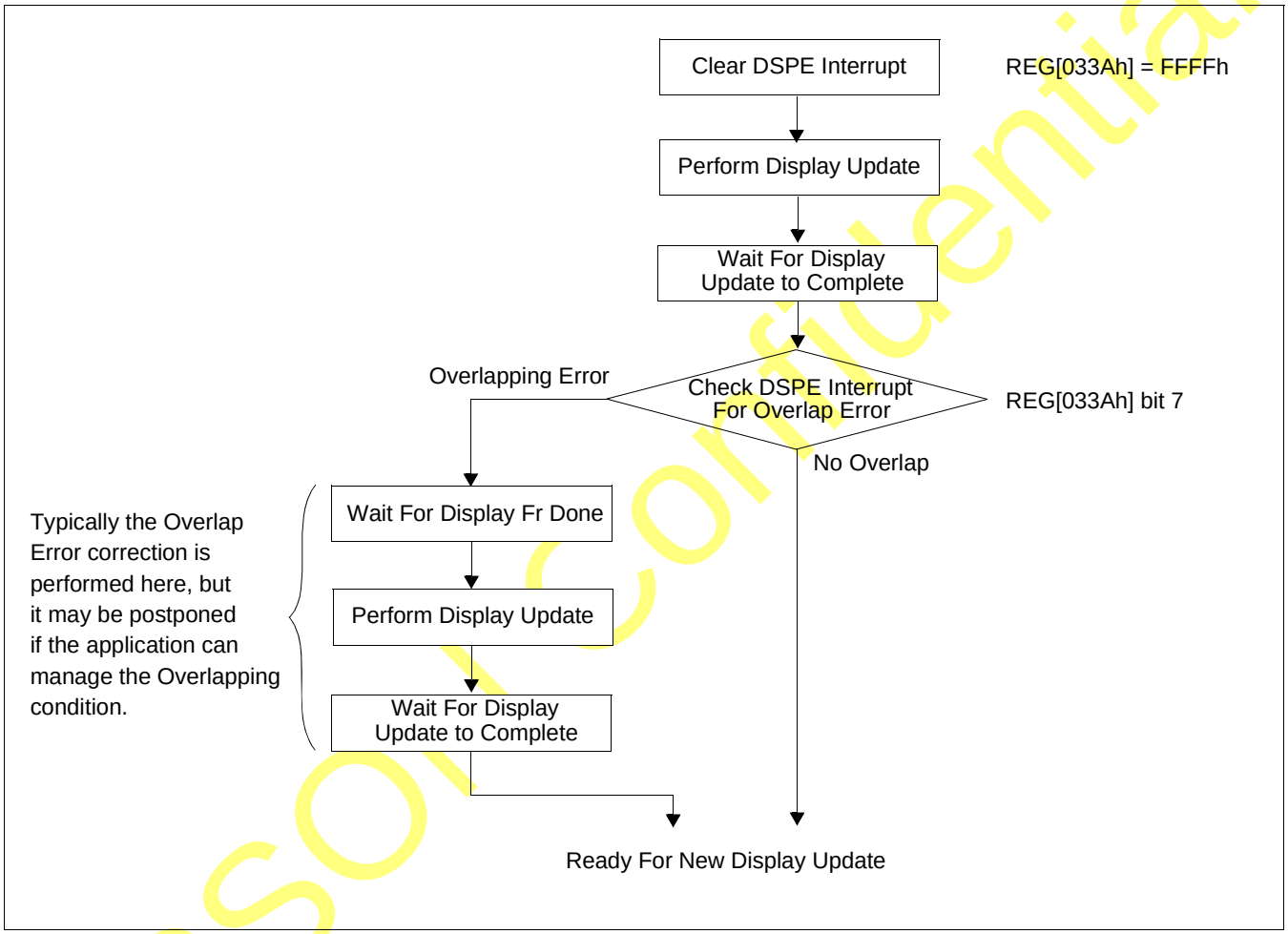


Figure 12-7: Overlapping Display Update Error Correction Programming Flow

12.6 Multi-Panel Support

The S1D13521 may be used to support a system with more than one panel when the following requirements are satisfied:

- Source and Gate Driver outputs are connected to an external buffer to guarantee drive strength.
- Only one panel is updated using the multi-LUT pipeline at a time.
- Memory includes a separate Image Buffer Area and Update Buffer Area for each panel.
- Shared Driver lines are properly connected
- Source Driver Chip Select lines are separate for each panel.

12.6.1 Source and Gate Driver Output Connections

The following diagram shows an example with three panels operated by a single S1D13521. Each panel requires three Source Drivers which are independently driven by the S1D13521 using 9 Source Driver Chip Select signals (SDCE_L[8:0]). The SDRAM memory includes a separate Image Buffer Area and Update Buffer Area for each panel.

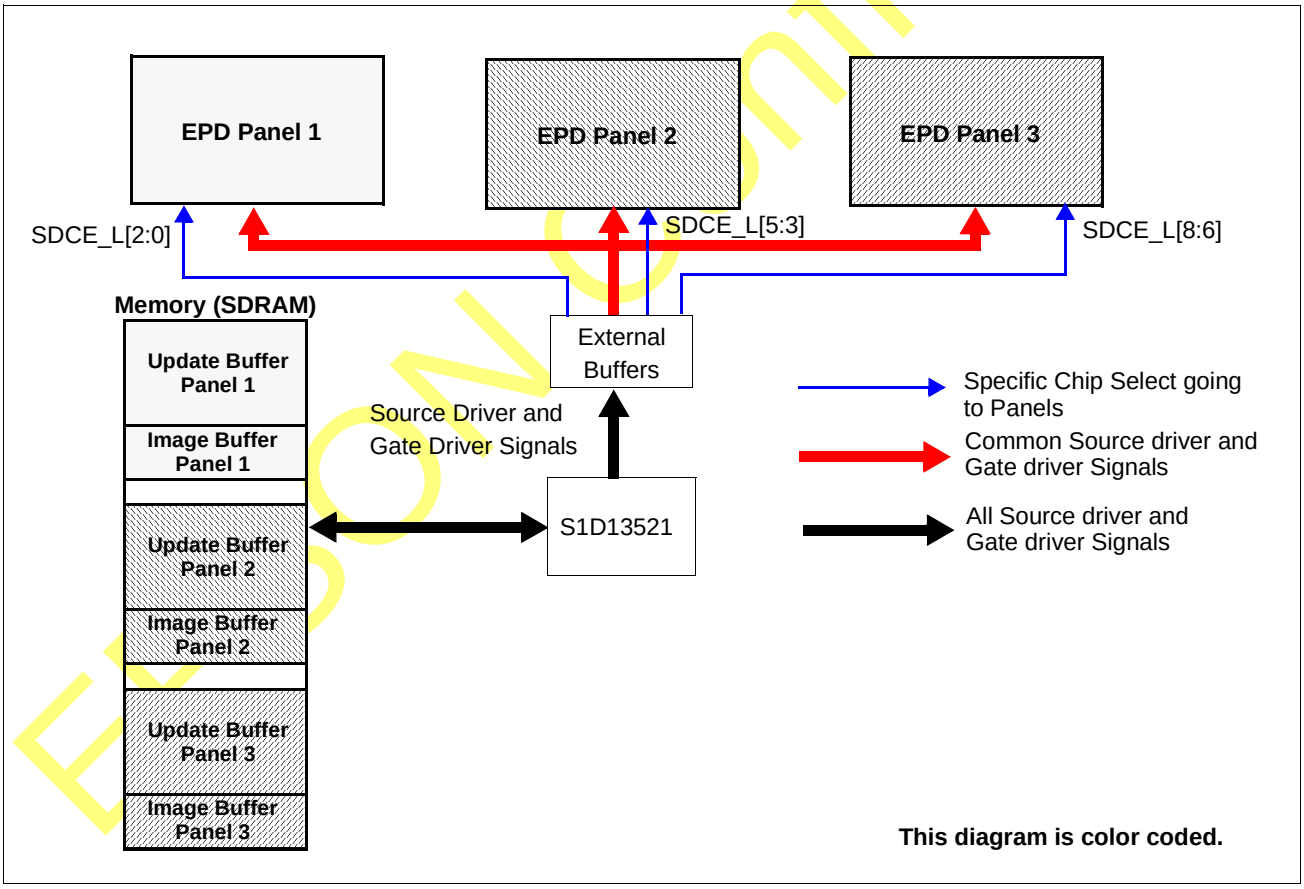


Figure 12-8: S1D13521 to Three Panel Connection Example

12.6.2 Configuration of Source Driver Chip Selects

The Source Driver Chip Select lines must be connected to the correct panel as switching between panels requires the Source Driver Chip Select Start bits to be properly selected. For a three panel example, the following configuration can be used.

EPD Panel 1 - uses Chip Selects 0, 1, and 2
EPD Panel 2 - uses Chip Selects 3, 4, and 5
EPD Panel 3 - uses Chip Selects 6, 7, and 8

When switching between which panel is driven, the Source Driver Chip Select Start bits in REG[030Ch] bits 15-12 must set as follows.

EPD Panel 1 - Uses Chip 0 to start, REG[030Ch] bits 15-12 = 000b
EPD Panel 2 - Uses Chip 3 to start, REG[030Ch] bits 15-12 = 011b
EPD Panel 3 - Uses Chip 6 to start, REG[030Ch] bits 15-12 = 110b

12.6.3 Switching Between Panels

When switching between which panel is driven, the following procedure is recommended.

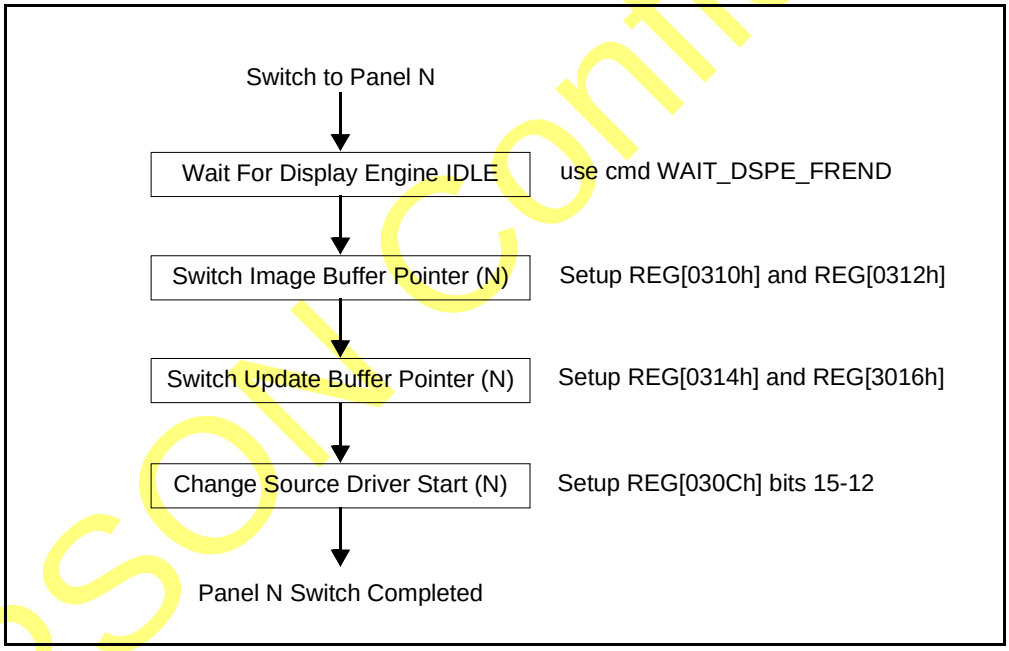


Figure 12-9: Switching Panel Driving Flow

12.7 Pop-Up Window Support

A Pop-Up Window overlays a new window (foreground image) on top of the currently displayed image (background image) without overwriting it. This function allows the background image to be restored without requiring the Host to rewrite the Image Buffer. Pop-Up Windows are implemented using two separate Image Buffers.

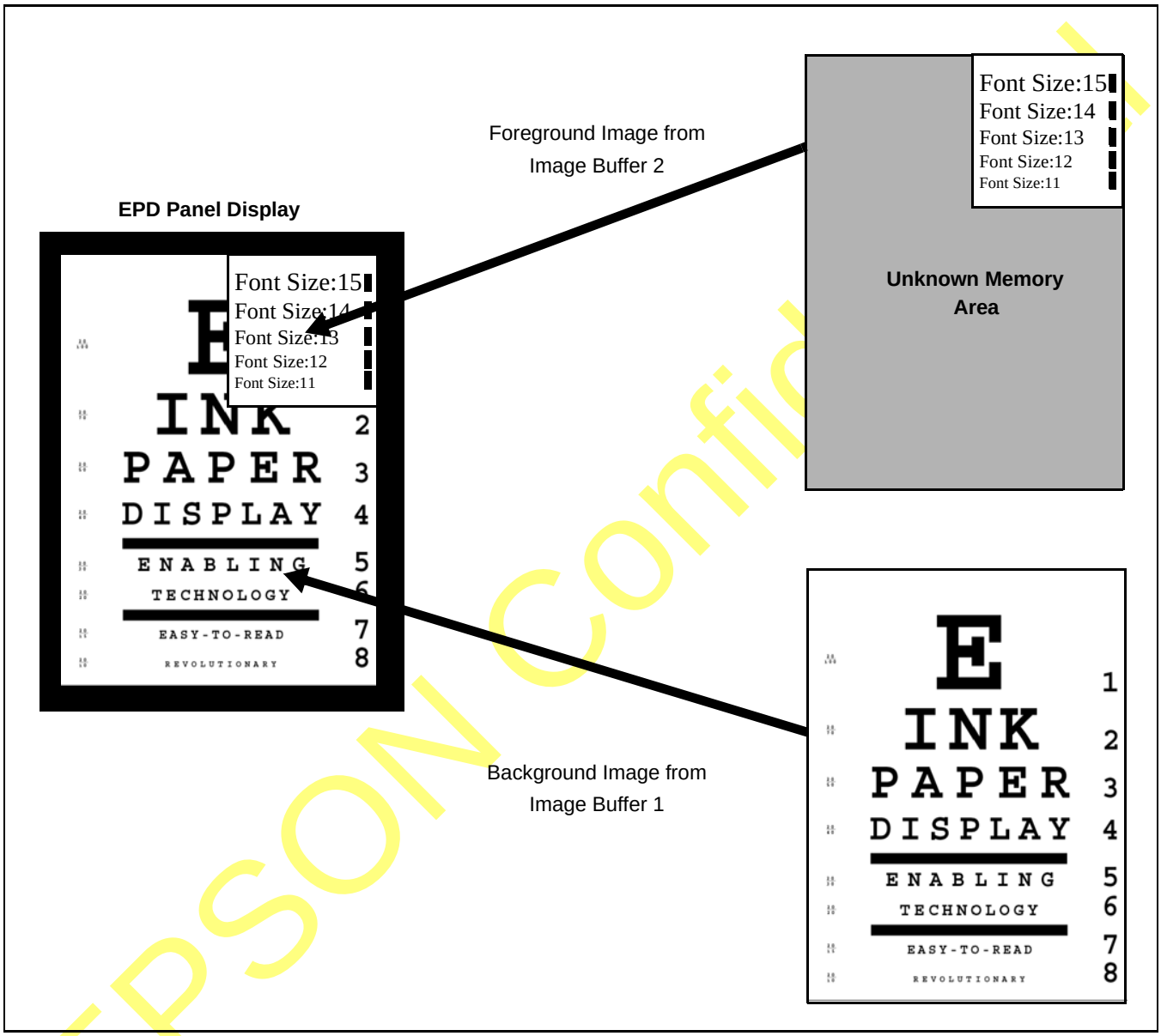


Figure 12-10: Pop-Up Window Example

12.7.1 Pop-Up Window Implementation

The S1D13521 can support multiple Image Buffers as described in 10.2.2, “Multiple Image Buffer Support” on page 82. Pop-Up Windows are supported using multiple Image Buffers and Regional Area Update mode (see UPD_FULL_AREA or UPD_FULL_PART commands).

A Pop-Up Window requires separate foreground and background Image Buffers. The foreground Image Buffer area does not need to contain image data for the full display area, only the display area that will be updated.

To create a Pop-Up Window, the following steps are recommended.

Step 1: Update the Background Image (full image update).

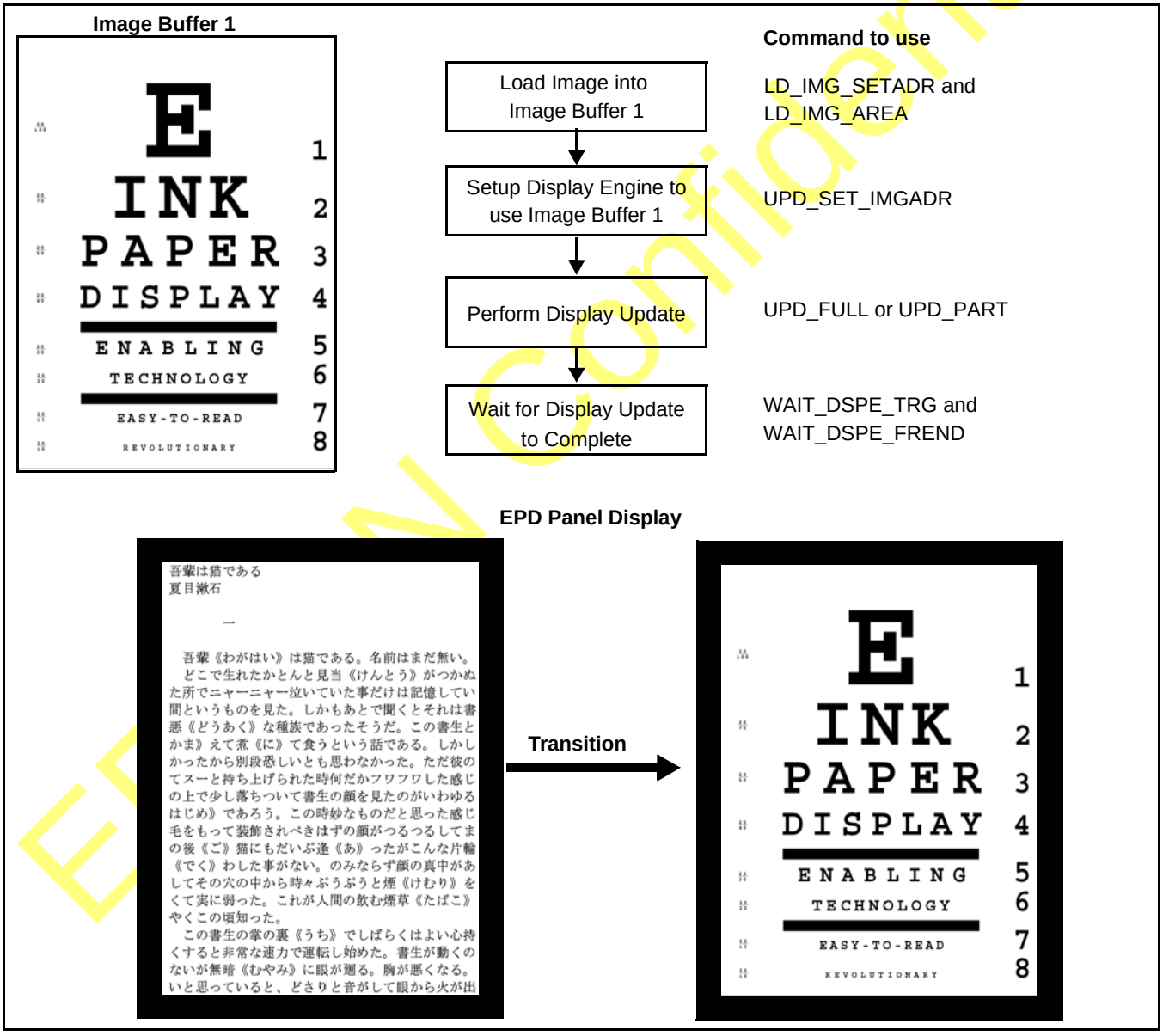


Figure 12-11: Creating a Pop-Up Window - Step 1

Step 2: Update the Foreground Image (partial update).

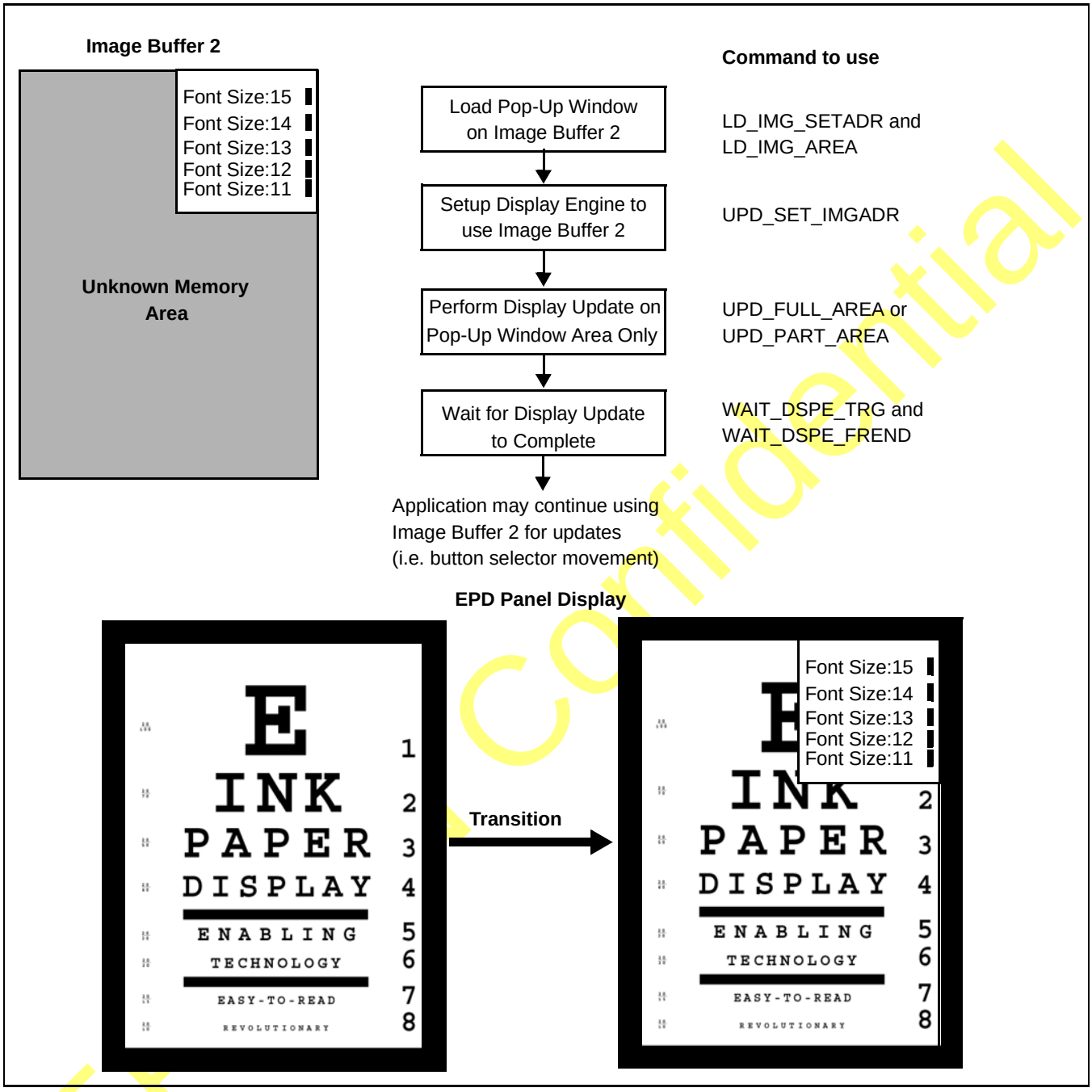


Figure 12-12: Creating a Pop-Up Window - Step 2

Step 3: Restoring the Background Image.

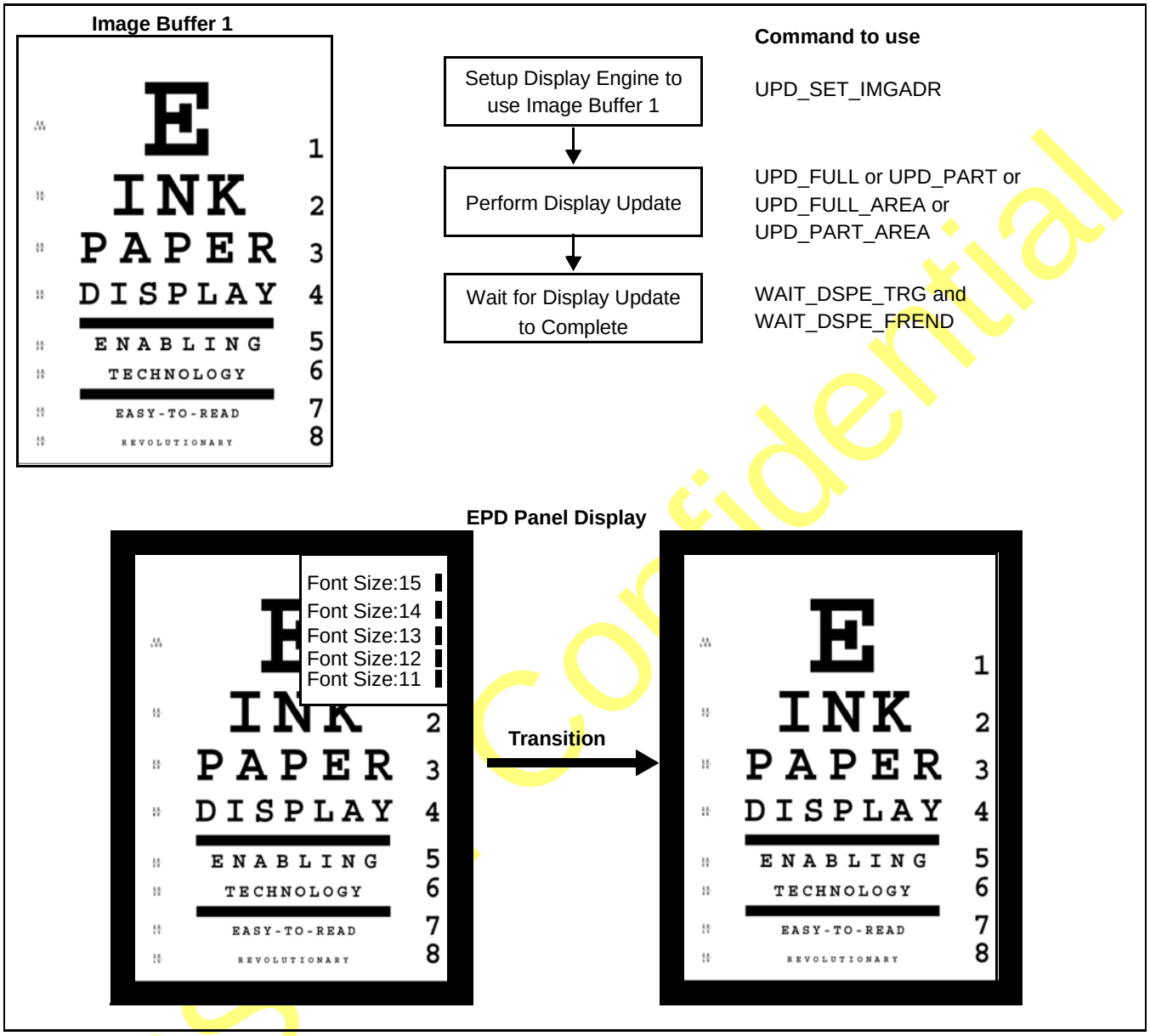


Figure 12-13: Creating a Pop-Up Window - Step 3

Chapter 13 SPI Interface

13.1 Register Descriptions

13.1.1 SPI Flash Chip Select Control Register

The SPI Flash Chip Select Enable bit (REG[0208h] bit 0) is used to assert/deassert the SPICS_L pin. The value programmed to this bit is the inverse of the SPICS_L output. The default value of this bit is 0b (SPICS_L = 1) which disables chip select.

13.1.2 SPI Flash Control Register

The SPI Flash Control Register (REG[0204h]) configures the operation of the SPI Flash Memory interface. It has the following control bits:

- Bit 0 is the SPI Flash Enable bit and is set to 1b to enable the SPI Interface.
- Bits 2-1 are the SPI Flash Clock Phase Select and SPI Flash Clock Polarity Select bits which select the SPICLK phase and polarity. For a summary of the phase and polarity settings, see Table 21-19 “SPI Flash Clock Phase and Polarity,” on page 186.
- Bits 5-3 are the SPI Flash Clock Divide Select bits for programming the SPICLK frequency.
- Bit 6 is the SPI Flash Read Command Select bit and is applicable only when bit 7 is 1b. It selects whether to use Normal Read or Fast Read commands when reading the Serial Flash Memory from the VBUS.
- Bit 7 is the SPI Flash Read Mode bit. When it is 0b, access to the external Serial Flash Memory is through firmware programming of the SPI registers. In this mode, control of the SPI interface engine is given to the SPI interface registers. When it is 1b, the Display Engine has control over the operation of Serial Flash Memory.

13.1.3 SPI Flash Write Data Register

This write only register (REG[0202h]) is used to trigger a byte serial transfer on the SPICLK/SPIO pins. Writing a byte value (with REG[0202h] bit 8 = 1b) to this register causes the byte value to be serial shifted out on SPICLK/SPIO.

13.1.4 SPI Flash Read Data Register

This read only register (REG[0200h]) is used to read byte data received from the SPI interface. In order to read a byte of data into this register, a “dummy” write to REG[0202h] must be performed (with REG[0202h] bit 8 = 0b).

13.1.5 SPI Flash Status Register

This read only register (REG[0206h]) provides status bits indicating the state of the SPI interface engine. The following status bits are available:

- Bit 0 is the SPI Flash Read Data Ready Flag. It is set to 1b whenever a new byte of data has been loaded into the SPI Flash Read Data register, REG[0200h]. This bit is cleared when REG[0200h] is read.
- Bit 1 is the SPI Flash Read Data Overrun Flag. It is set to 1b whenever a new byte of data is loaded into the SPI Flash Read Data register, REG[0200h], and the SPI Flash Read Data Ready Flag (bit 0) is still 1b (indicating that the previous byte has not yet been read out). This bit is cleared by reading REG[0200h].
- Bit 2 is the SPI Flash Write Data Register Empty Flag. It is set to 1b whenever the SPI Flash Write Data Register, REG[0202h], is empty. Writing a byte value to REG[0202h] will initially cause this bit to return 0b. When the byte value is transferred to the serial shift register, this bit is set to 1b again.
- Bit 3 is the SPI Flash Busy Flag. It is set to 1b when the SPI interface engine is busy shifting a byte of data in/out on the SPI interface.

13.2 Flash Memory Accesses using SPI Interface Registers

The following figures show the recommended sequences for accessing the Serial Flash Memory using the SPI interface registers. Before performing instruction sequences, the SPI interface must be configured using the SPI Flash Control Register, REG[0204h]. A Write Enable instruction sequence must have been executed before any Page Program instruction sequence.

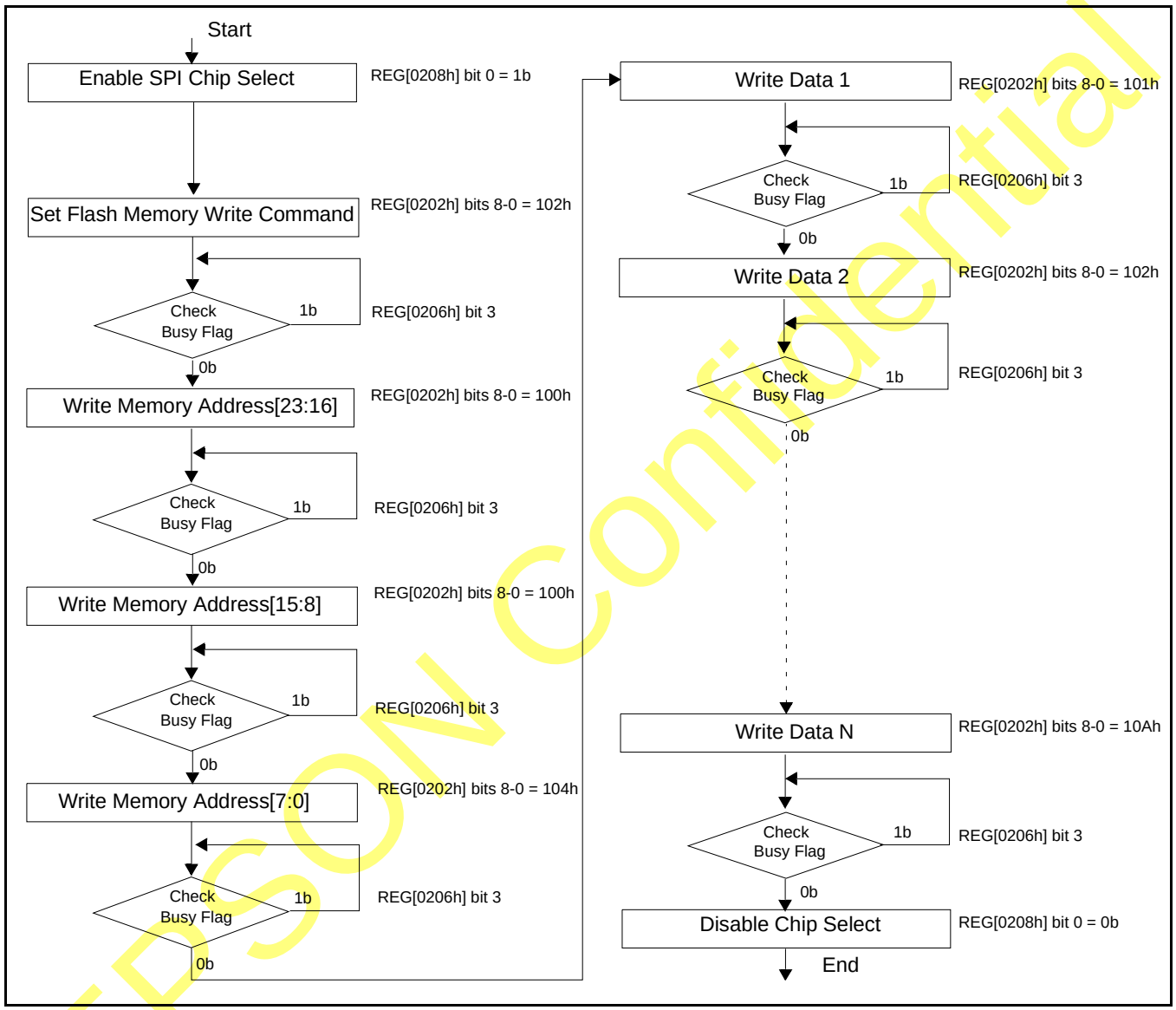


Figure 13-1: Page Program (Write Data) Instruction Sequence

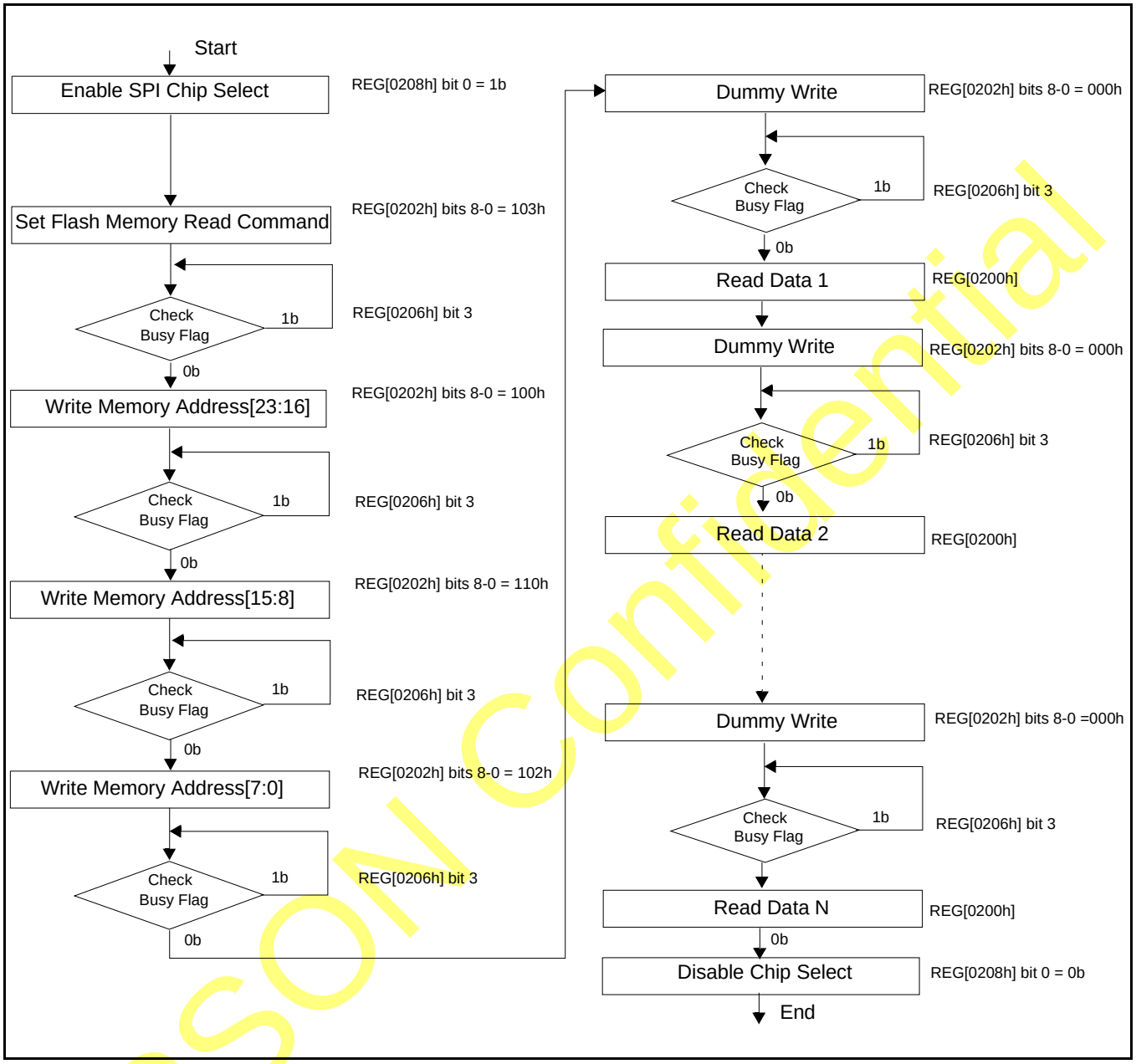


Figure 13-2: Read Data Instruction Sequence

Chapter 14 Firmware Programming Guide

14.1 Command Based Programming

The following sections contain programming sequences for:

- Initializing and Programming a Blank Serial Flash
- Power On Initialize to a Known State (Stored Image)
- Standby Mode
- Sleep Mode
- Sleep Mode
- Run Mode
- Host Packed Pixel Write
- Host Area Defined Packed Pixel Write
- Display Engine - Gate Driver Clear Request
- Display Engine - Update Buffer Initialize with Image Buffer
- Display Engine - Full Display Update - Full Image Size Sweep
- Display Engine - Partial Display Update - Full Image Size Sweep
- Display Engine - Partial Display Update - User Defined Area Sweep

Note
When using the internal oscillator (CNF2=1), there are timing requirements that must be observed or the Command Interface hardware will not be able to perform a normal boot-up initialization sequence which will result in a system failure for the S1D13521. For details on these timing requirements, refer to Chapter 18, “OSC Clock Timing Requirements” on page 145.

14.1.1 Initializing and Programming a Blank Serial Flash

The external Serial Flash memory must be programmed with the correct contents from address 0x000 ~ 0x885 of the serial flash. The command interface cannot operate without the Serial Flash containing the correct instruction codes. When the Serial Flash contents are invalid, only 2 commands are available:

0x10 - Command Read Register
0x11 - Command Write Register

For the recommended Serial Flash Contents, please contact your Epson sales office.

The following programming flow is recommended.

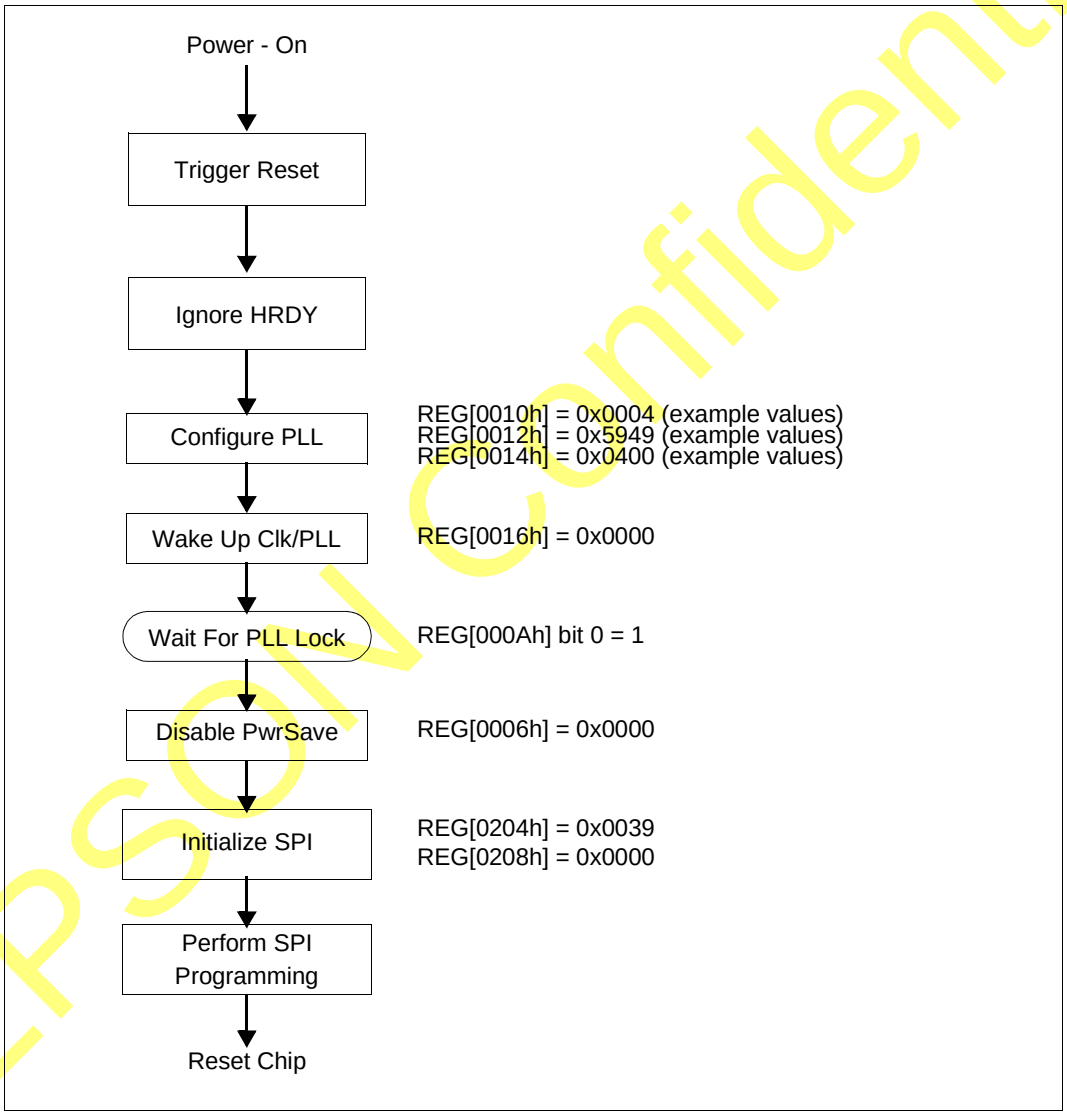


Figure 14-1: Initializing and Programming a Serial Flash Programming Flow

14.1.2 Power On Initialize to a Known State (Stored Image)

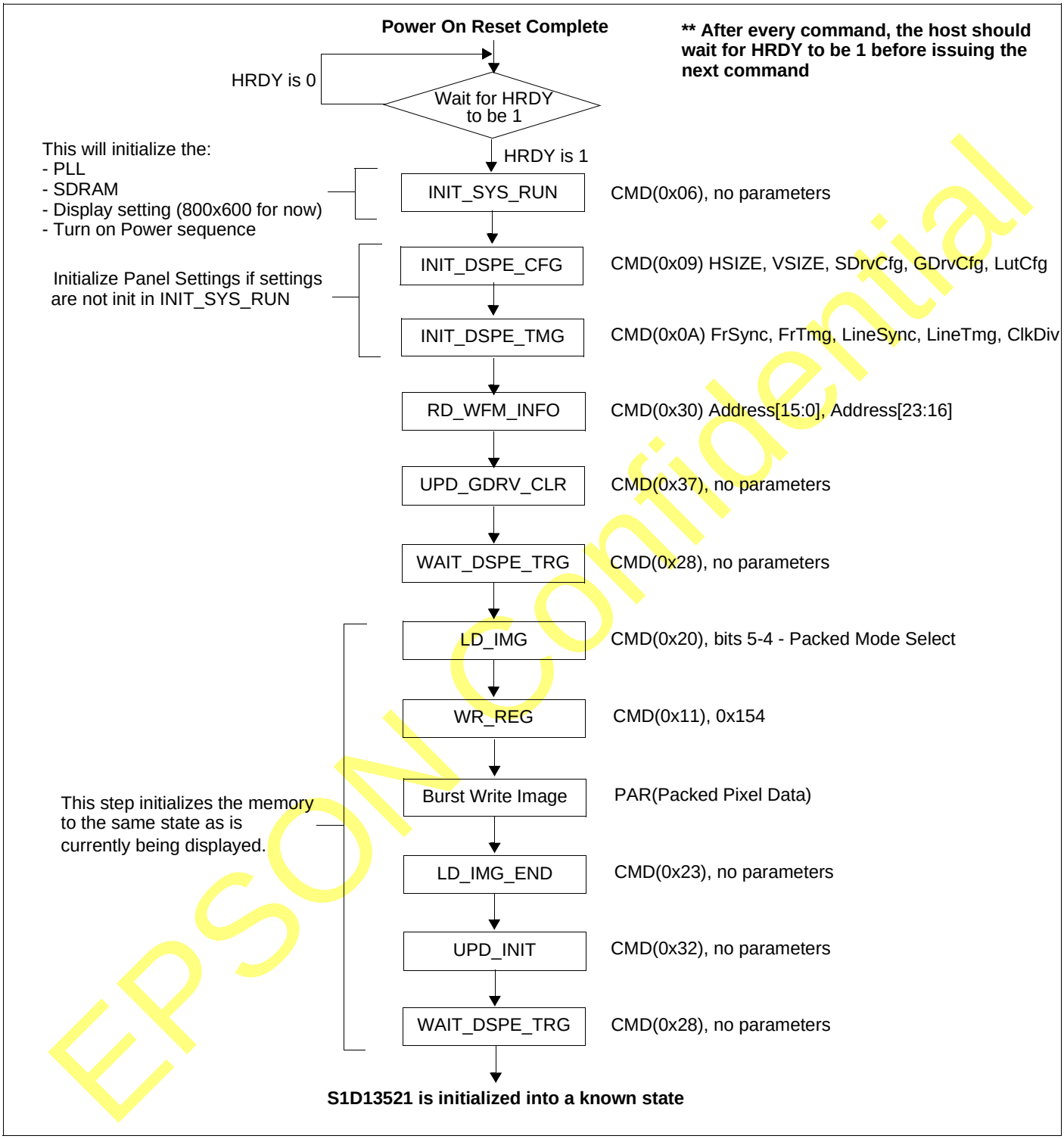


Figure 14-2: Power On Initialize to a Known State Programming Flow

14.1.3 Standby Mode

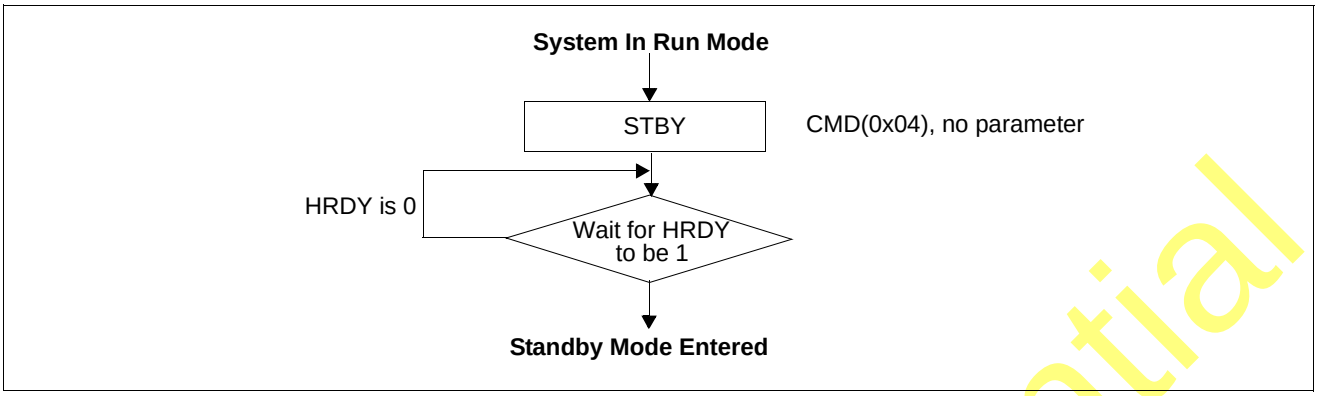


Figure 14-3: Standby Mode Programming Flow

14.1.4 Sleep Mode

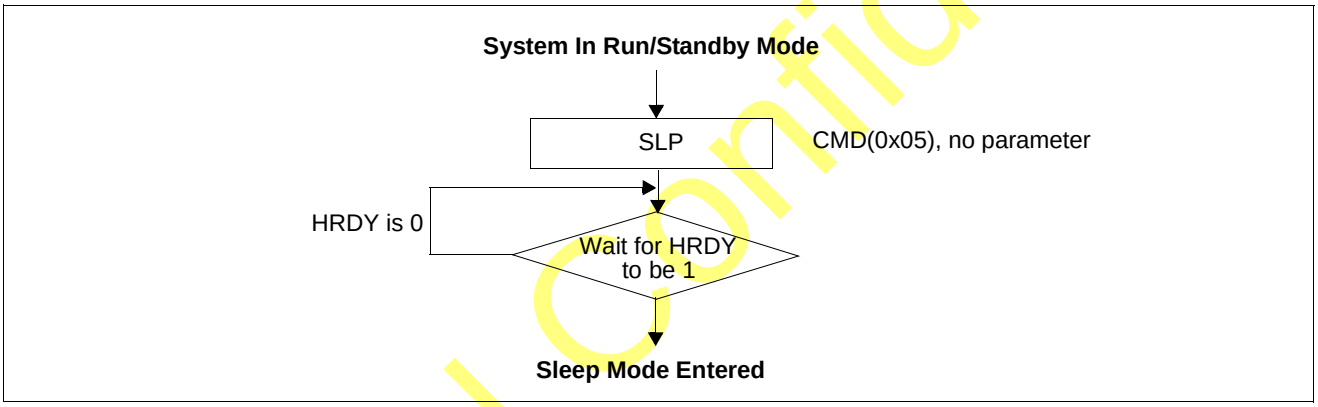


Figure 14-4: Sleep Mode Programming Flow

14.1.5 Run Mode

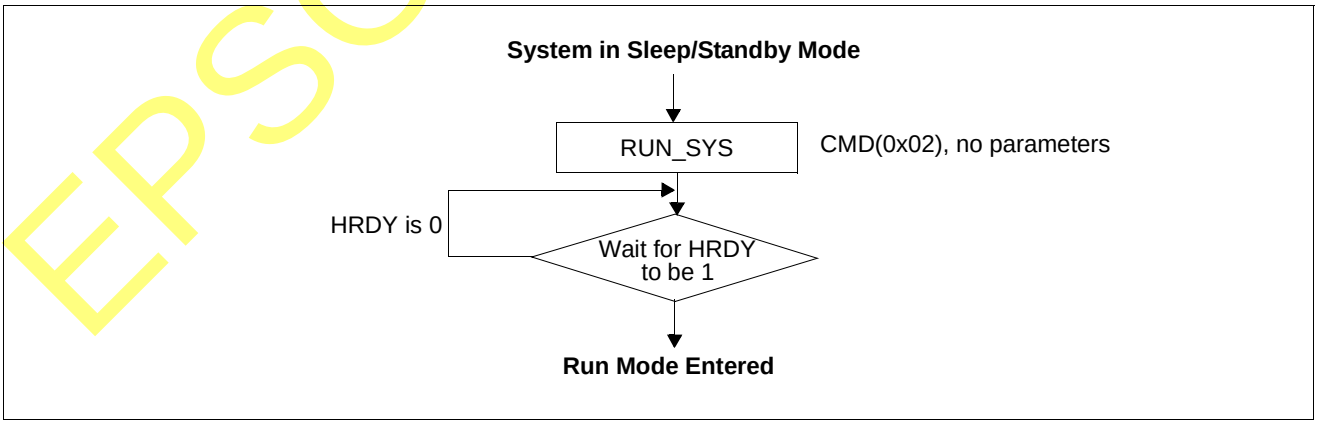


Figure 14-5: Run Mode Programming Flow

14.1.6 Host Packed Pixel Write

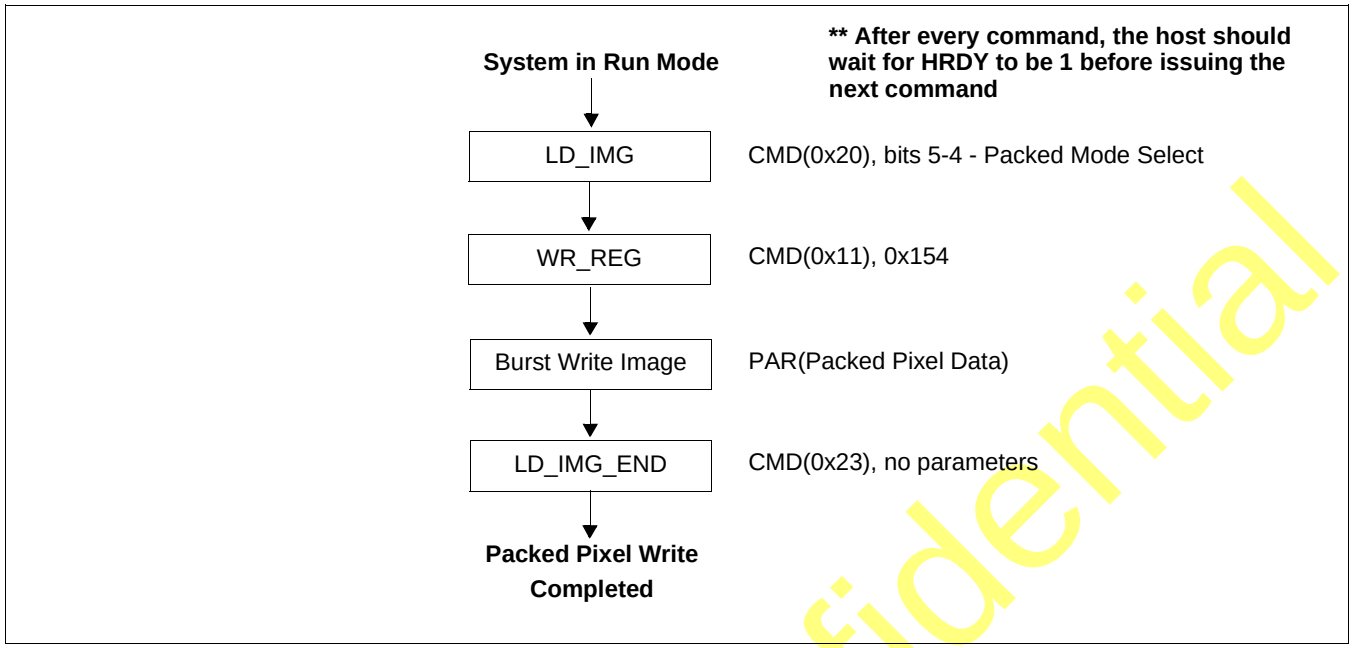


Figure 14-6: Host Packed Pixel Write Programming Flow

14.1.7 Host Area Defined Packed Pixel Write

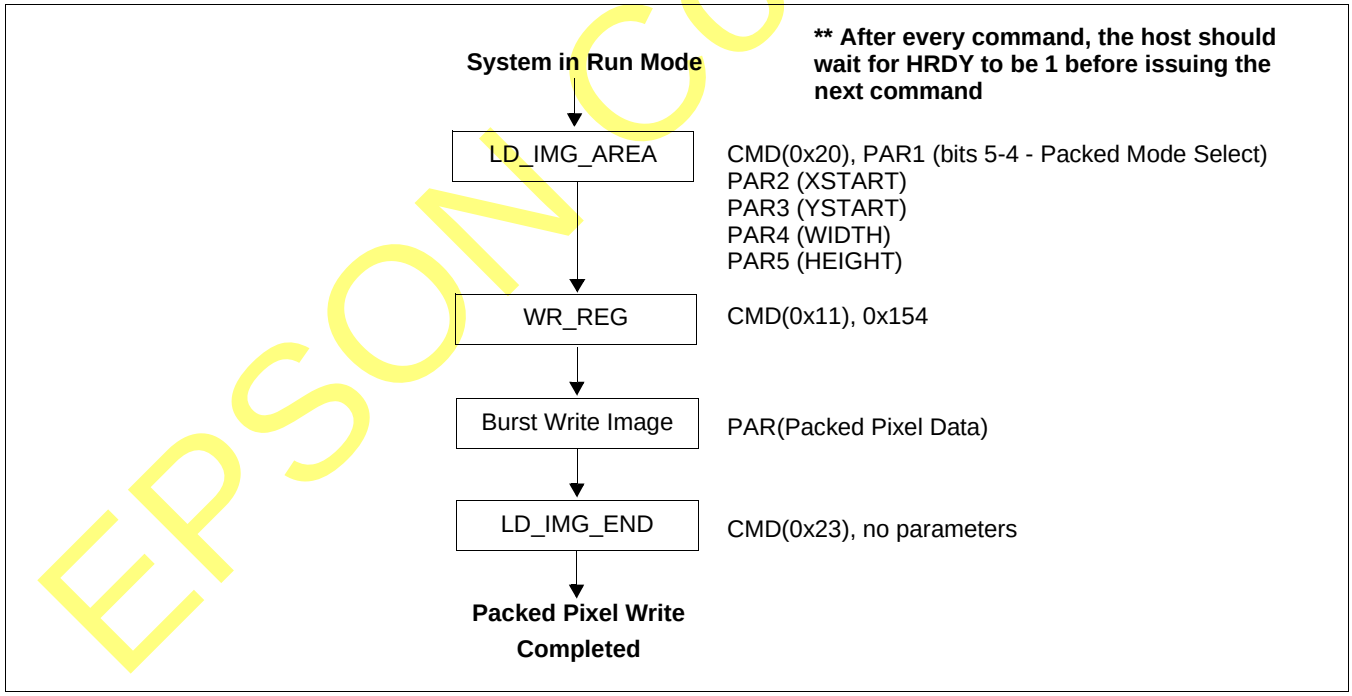


Figure 14-7: Host Area Defined Packed Pixel Write Programming Flow

14.1.8 Display Engine - Gate Driver Clear Request

This sequence is used on power up when the gate driver must be set to a known state.

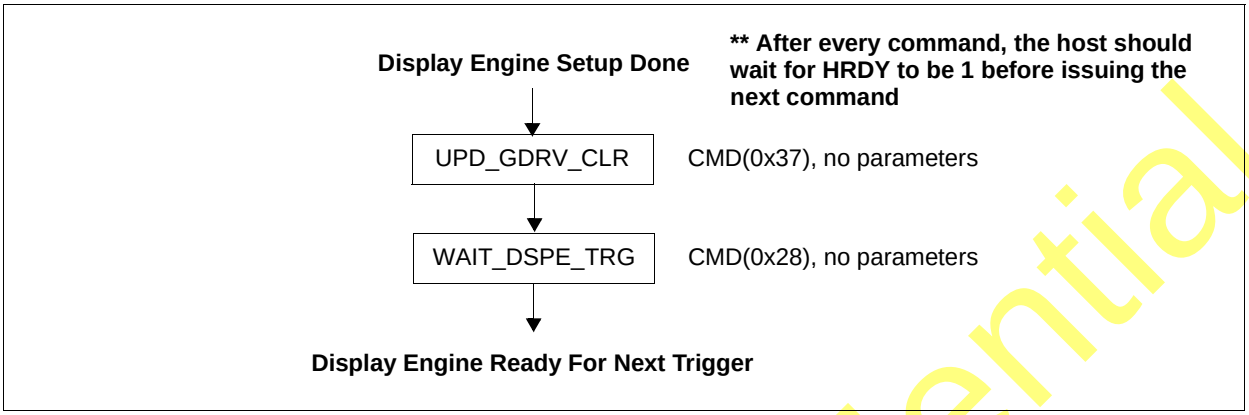


Figure 14-8: Display Engine - Gate Driver Clear Request Programming Flow

14.1.9 Display Engine - Update Buffer Initialize with Image Buffer

This sequence will initialize the update buffer without display output.

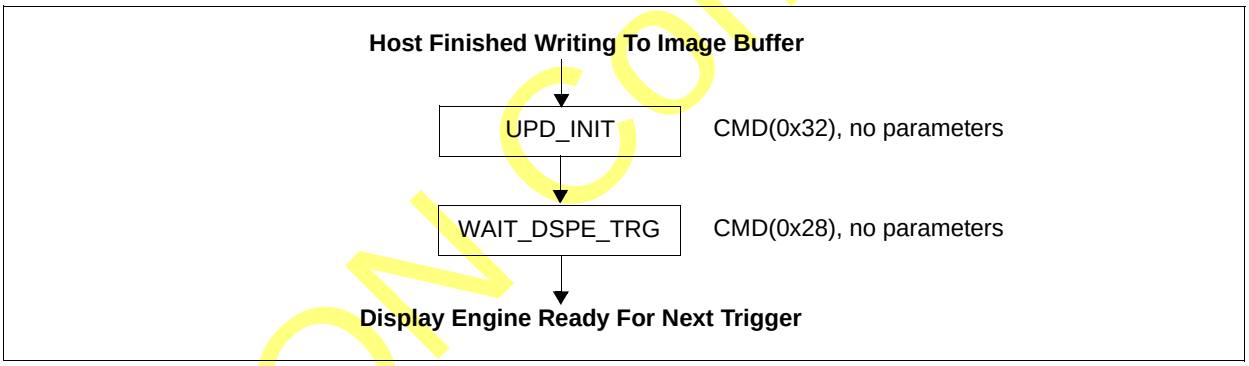


Figure 14-9: Display Engine - Update Buffer Initialize with Image Buffer Programming Flow

14.1.10 Display Engine - Full Display Update - Full Image Size Sweep

This operation forces a display update for every pixel within the defined display size, regardless of whether the pixel data has changed.

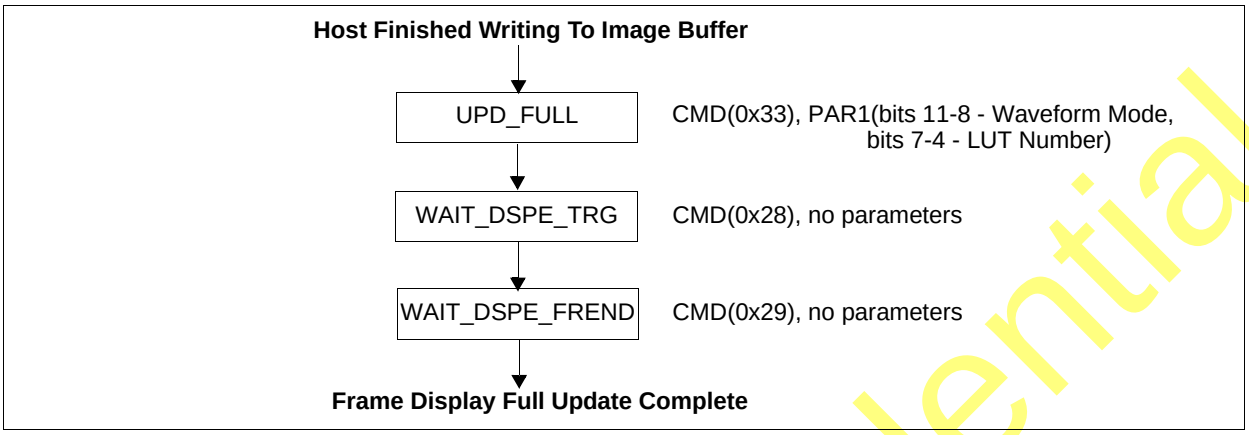


Figure 14-10: Display Engine - Full Display Update - Full Image Size Sweep Programming Flow

14.1.11 Display Engine - Full Display Update - User Defined Area Sweep

This operation forces a display update for every pixel within the user defined area, regardless of whether the pixel data has changed.

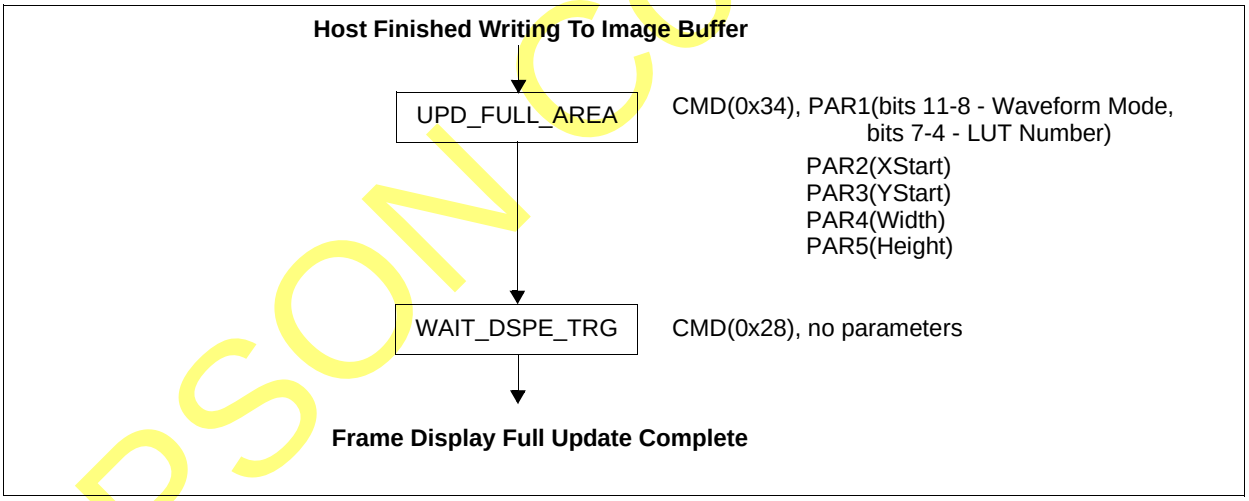


Figure 14-11: Display Engine - Full Display Update - User Defined Area Sweep Programming Flow

14.1.12 Display Engine - Partial Display Update - Full Image Size Sweep

This operation performs a display update for every pixel with changed pixel data within the defined display size.

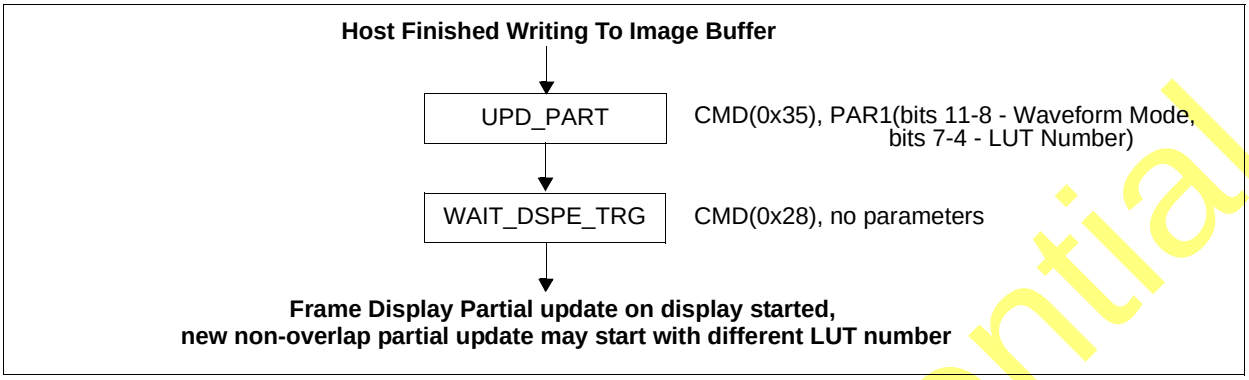


Figure 14-12: Display Engine - Partial Display Update - Full Image Size Sweep Programming Flow

14.1.13 Display Engine - Partial Display Update - User Defined Area Sweep

This operation performs a display update for every pixel with changed pixel data within the user defined area.

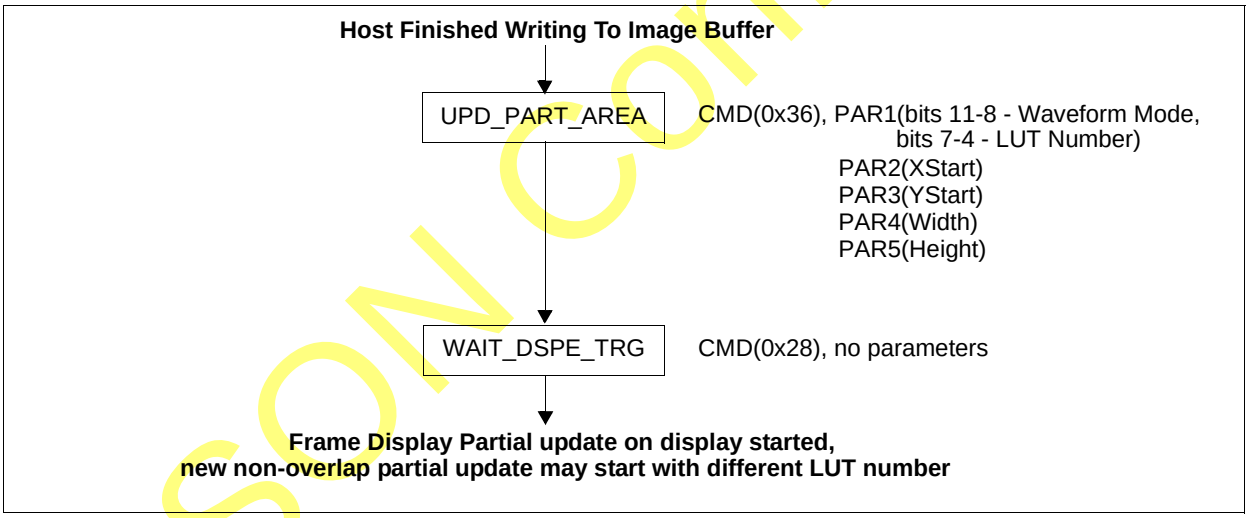


Figure 14-13: Display Engine - Partial Display Update - User Defined Area Sweep Programming Flow

14.1.14 Manual Trigger to I2C Thermal Sensor for Single Temperature Read

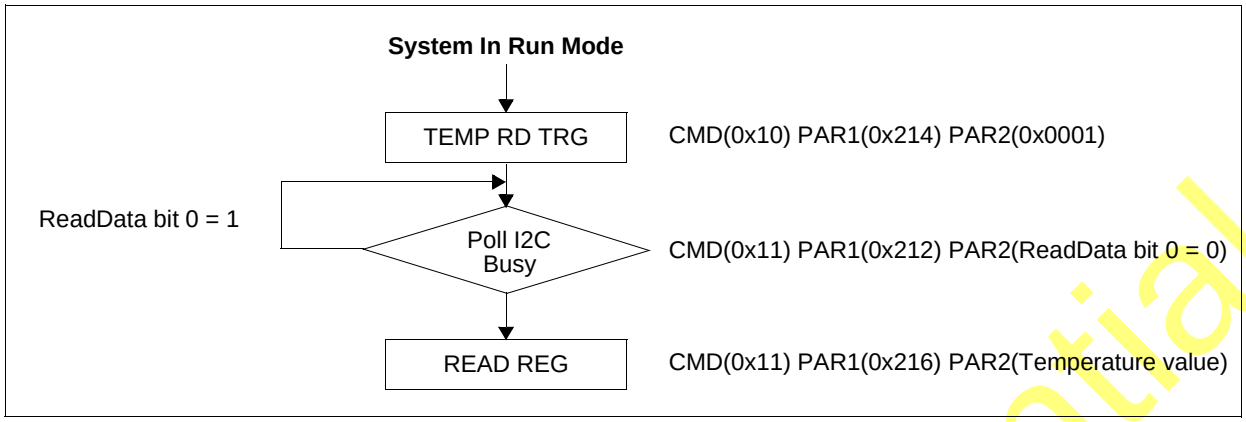


Figure 14-14: Manual Trigger I2C Thermal Sensor for Single Temperature Read Programming Flow

14.1.15 Full Image Buffer Dump (Byte Data Only)

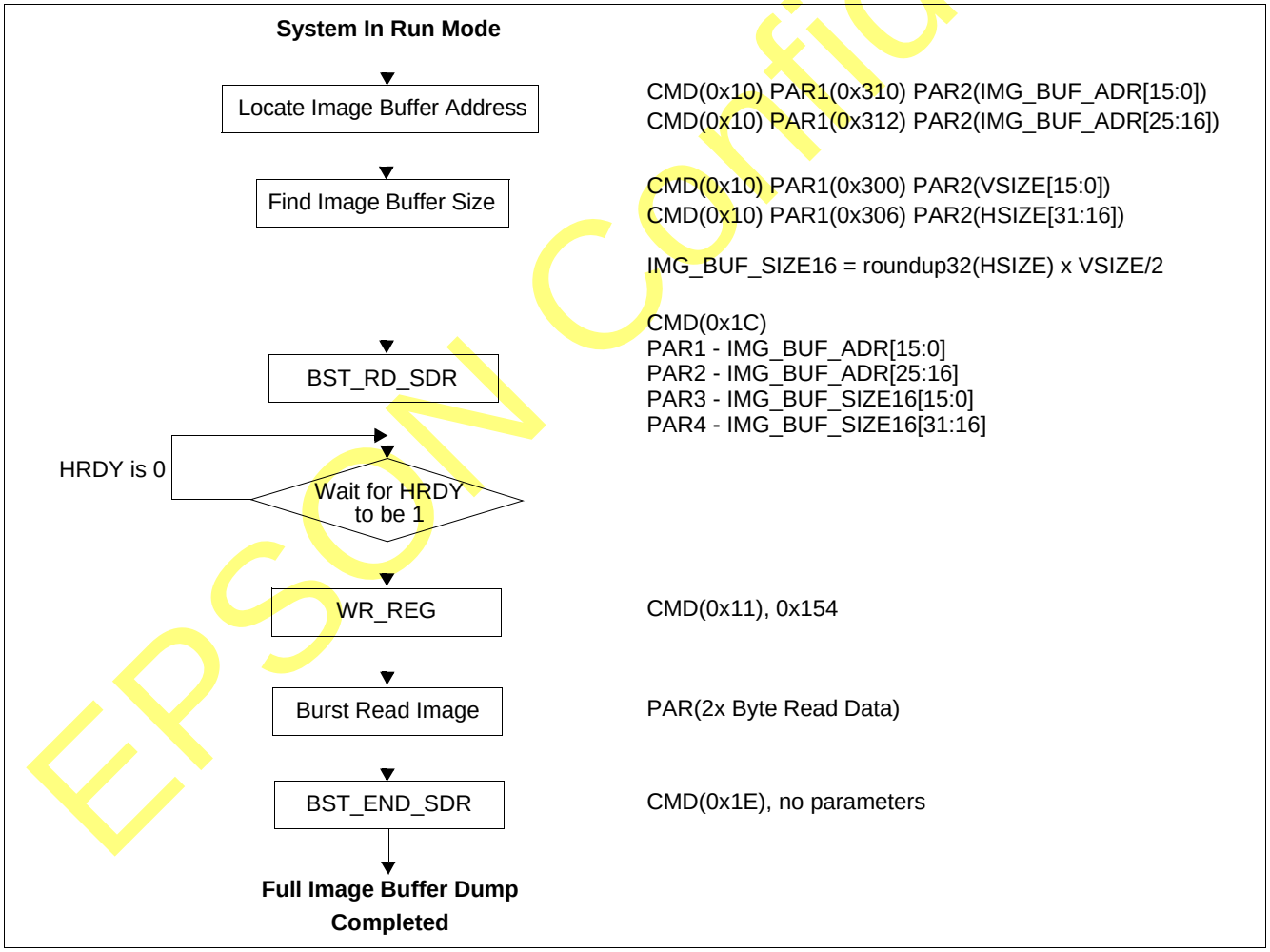


Figure 14-15: Full Image Buffer Dump (Byte Data Only) Programming Flow

Chapter 15 Auto Waveform Mode

15.1 Introduction

E Ink has developed several waveforms which are optimized to efficiently display different grey-tones in the shortest possible time. Some of these waveforms are actually a subset of the general purpose waveforms.

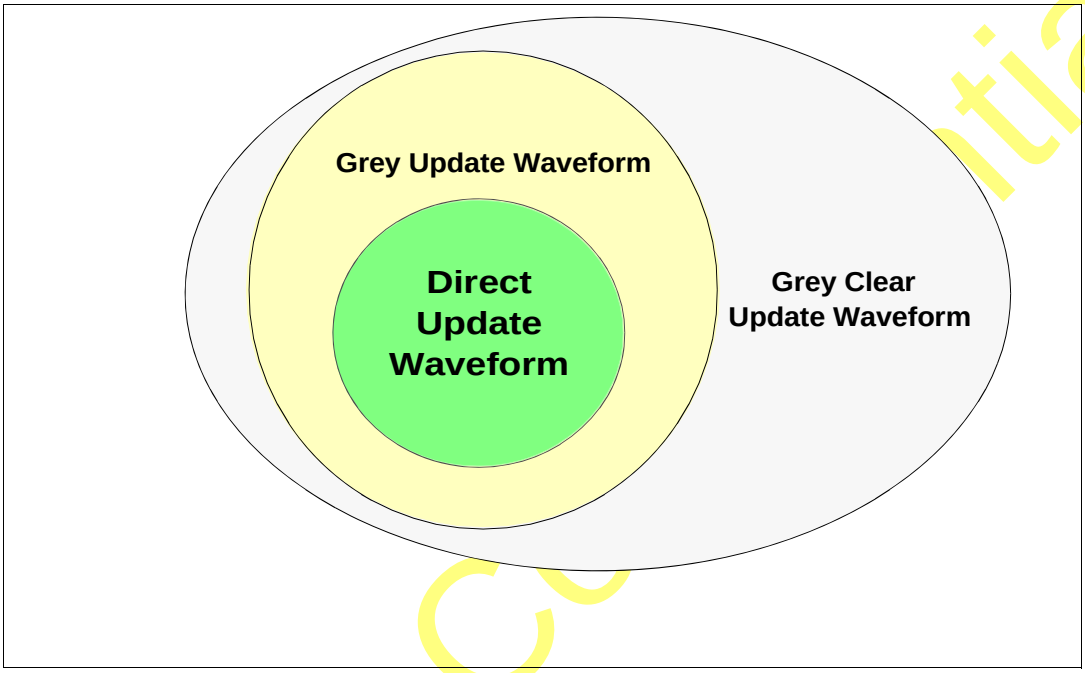


Figure 15-1: Waveform Example Sets

In the above example, the Grey Update and Grey Clear Waveforms can be used for grey-toned pixel updates and require approximately 780 ms for the pixel update to complete. The Grey Update Waveform is able to perform a pixel transition with minimal flashing behavior on the panel. The Grey Clear Update Waveform exhibits flashing behavior to reset the pixel grey level to a known state, removing any build up compounded error from previous operations.

The Direct Update Waveform is a subset of the Grey Update Waveform. The Direct Update Waveform can be used to convert any grey-toned pixel to a black or white level in approximately 260 ms.

Typically, an application manages which waveform should be used as it knows the contents that will be displayed. In cases where the application doesn't manage the contents that will be displayed, due to multiple layers of program architecture, Auto Waveform Mode may be configured to automatically select the best waveform to use.

15.2 Architecture

The Auto Waveform Mode engine contains four priority pixel comparator logics (Compare 0, 1, 2 and 3), where Compare 0 has the highest priority and Compare 3 has the lowest priority. When all four compares register as invalid, an Auto Waveform Mode Error is set in REG[033Ah] bit 14. The comparisons are performed on a per pixel basis during frame update trigger operations. All pixels which will require updates must conform to the compare # logic requirement.

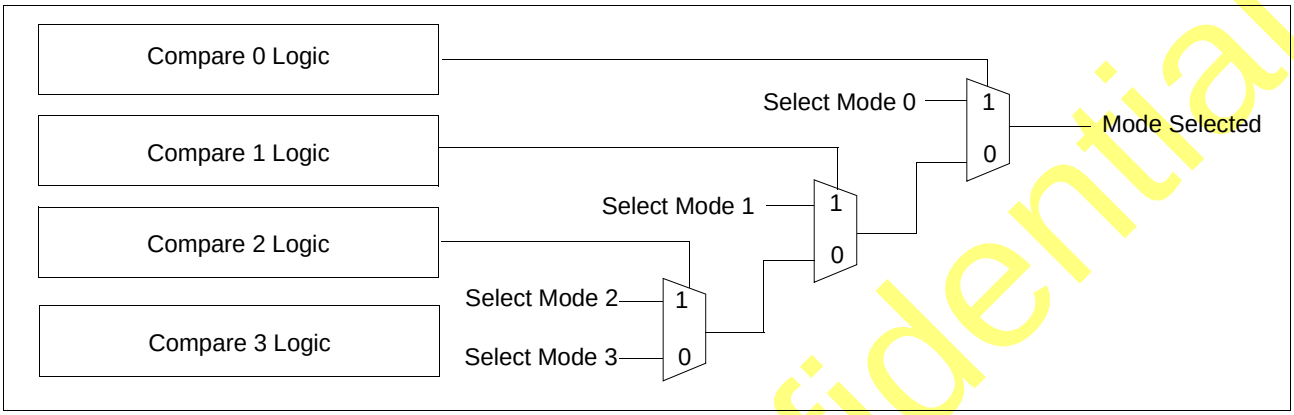


Figure 15-2: Auto Waveform Priority Logic

Each Compare Logic has independent configuration settings for the following:

- Pixel Change Minimum Threshold (0-255)
  This setting is always enabled and defines the minimum pixel value difference between the current pixel and the next pixel. The pixel change value must be equal to or greater than the threshold limit.
- Current Pixel Value with Compare Enable
  This setting can be enabled or disabled. When enabled, the current pixel value is compared with the current pixel compare value. The current pixel value must match this value.
- Next Pixel Value with Compare Enable
  This setting can be enabled or disabled. When enabled, the next pixel value is compared with the next pixel compare value. The next pixel value must match this value.
- Mode number select (0-15).
  This setting must be set to select the appropriate Waveform from the E Ink set of waveforms.

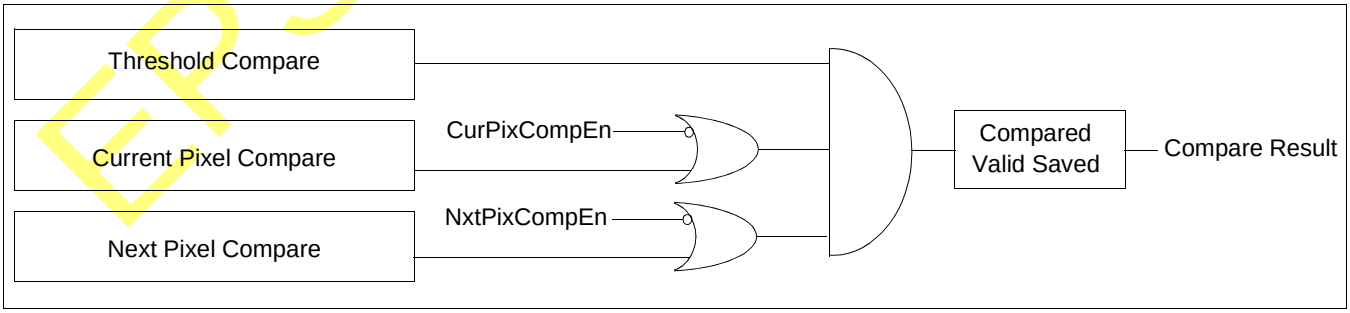


Figure 15-3: Single Compare Logic

15.3 Auto Waveform Mode Example Setup

In this example, the waveform is selected from either the Grey Clear Update Waveform, Grey Update Waveform, or Direct Update Waveform. Each waveform has the following characteristics.

- Grey Clear Update Waveform
  This waveform is used for grey-toned pixel updates and requires approximately 780 ms for the pixel update to complete. This waveform differs from the Grey Update Waveform as it refreshes the pixel level to reduce ghosting from cumulative pixel transition error from the previous update operation.
- Grey Update Waveform.
  This waveform is used for grey-toned pixel updates and requires approximately 780 ms for the pixel update to complete. This waveform provides high quality with a minimal flashing behavior which may not reduce ghosting and may add cumulative pixel transition error.
- Direct Update Waveform
  This waveform is used to convert grey-toned pixels to either a black or white level and requires approximately 260 ms. This waveform provides a fast pixel level change to black or white.

From the characteristics described above, the most desirable waveform to use is the Direct Update Waveform, followed by the Grey Update Waveform, and lastly the Grey Clear Update Waveform. Based on these considerations, the Auto Waveform Update configuration should be set as follows.

Table 15-1: Compare Logic Settings

Compare Logic #	Pixel Change Threshold	Current Pixel Compare	Next Pixel Compare	Waveform To Use
0	10h	Disable	F0h	Direct Update
1	10h	Disable	00h	Direct Update
2	10h	Disable	Disable	Grey Update
3	n/a	n/a	n/a	Grey Clear Update

Note
The setting above is based on Display Engine LUT mode P4N (REG[0330h] bits 2-0 = 100b) where only the 4-bit MSB of the byte setting is used.

Direct Updates must occupy 2 compare logic levels. Compare Logic 0 is configured to detect grey-tone to white transitions. Compare Logic 1 is configured to detect grey-tone to black transitions. The Pixel Change Threshold should be set to 10h so that it will only register a pixel change when there is a minimum of one pixel level change transition.

Grey Update occupies Compare Logic 2, where it detects any change in pixel level. The Pixel change Threshold should be set to 10h to detect a minimum of 10h level change.

Grey Clear Update is the lowest priority at Compare Logic 3. For Grey Clear Updates only, the Pixel Change Threshold should be set to 0h. This way when a full update is requested without a pixel level change, this compare logic will be activated to use Grey Clear Update Waveform to refresh the display with no ghosting.

Chapter 16 Waveform Modes

E Ink waveforms are optimized for each specific panel model. For details on the specific waveforms for each panel, contact your E Ink representative.

The following table lists some example waveform modes available for E Ink panels.

Table 16-1 : WD (3-bit) Typical Performance

Mode	Mode	Type	Grey Levels	Transition Appearance	Ghosting	Usage	Target Update Time at 25°C (ms)
INIT	0	Global	White only	High Flash	n/a	Display Initialization	~4000
DU	1	Local	8 → Black and White	No Flash	Low	Monochrome menu, text input, touch screen/pen input	260
GU	2	Local	8	Low Flash	Medium	High quality images and anti-aliased text	780
GC	3	Global	8	High Flash	Low	High quality images and anti-aliased text	780

Note
The waveform specification is only available to end customers who have entered a non-disclosure agreement with E Ink.

Chapter 17 External Components

The S1D13521 can be connected to a number of external devices. The following sections provide recommendations for implementing these devices.

17.1 OSC Circuit

The S1D13521 includes a 2-terminal crystal interface for the internal oscillator. When a crystal is used, the following recommendations must be observed.

- the crystal must be placed close to the chip
- the crystal must be surrounded by a ground barrier
- the crystal must not have any other signals routed through it

The following figure shows an example OSC circuit.

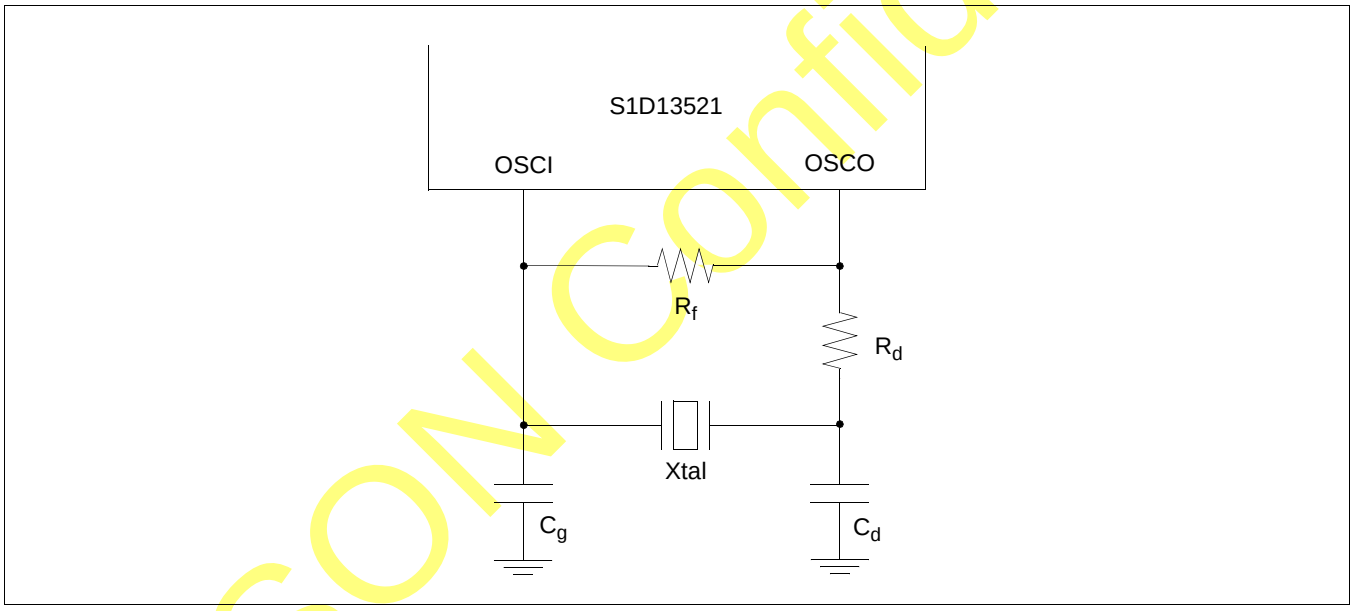


Figure 17-1: Example OSC Circuit

Table 17-1 Recommended Oscillator External Circuit Parameter

Symbol	Parameter	Min	Typ	Max	Units
R_f	Rf	—	1	—	MΩ
R_d	Rd	—	220	—	Ω
C_g	Cg	—	30	—	pF
C_d	Cd	—	30	—	pF
Xtal	Fundamental mode Crystal	25	—	26.5	MHz

17.2 LM75 Compatible Thermal Sensor

The S1D13521 supports the I2C sequences necessary for performing temperature readings from a National LM75 Digital Temperature Sensor or compatible device. The thermal sensor must meet the following requirements.

Table 17-2: LM75 Compatible Requirements

Parameter	Requirements
Interface Support	I2C (400kbit/s or 3.4Mbit/s)
Temperature Range	-25^{o}C to 80^{o}C in 1 Degrees increment
I2C Operation	Address Byte + 1 Temperature Byte

For detailed information on the LM75, refer to the National Semiconductor webpage at www.national.com.

17.2.1 Thermal Sensor Connection Example

The following figure shows an example implementation for connecting the S1D13521 to a Thermal Sensor.

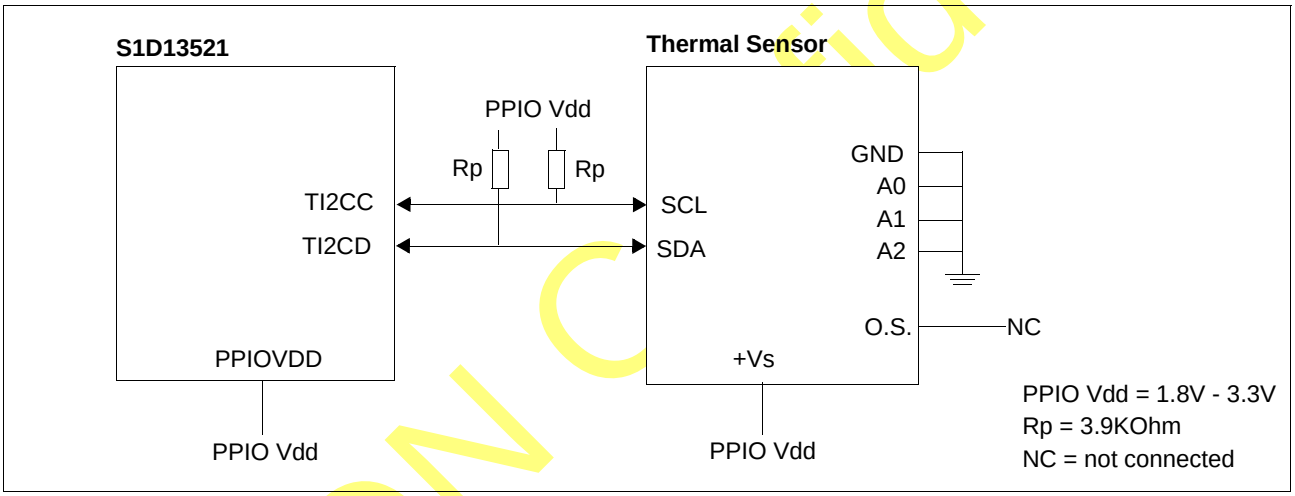


Figure 17-2: Example Thermal Sensor Connection

17.2.2 Thermal Sensor Operation Timing

A single temperature retrieval operation will always consist of 4 operations in the following order.

- Start Sequence
- Address Byte
- Temperature Byte retrieval
- Stop Sequence

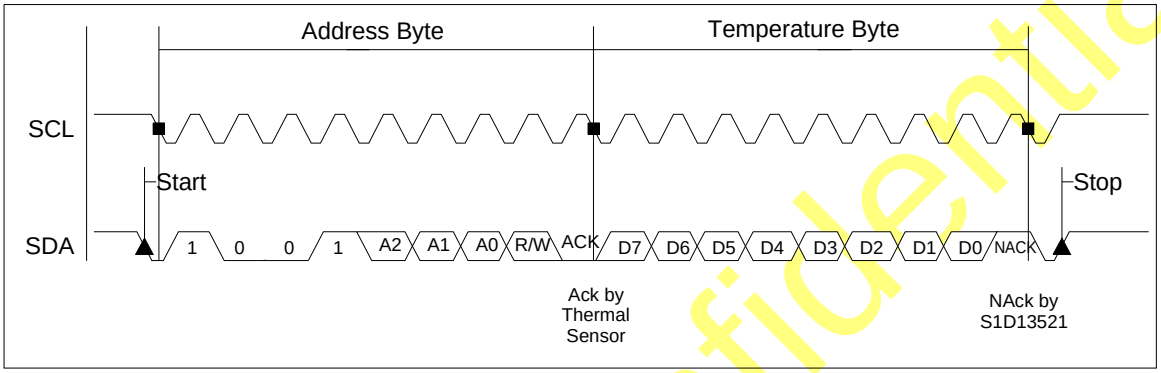


Figure 17-3: Thermal Sensor Operation Timing

For an example sequence to perform a single temperature read using Command based programming, see 14.1.14, “Manual Trigger to I2C Thermal Sensor for Single Temperature Read” on page 128.

17.3 Serial Flash Memory

The S1D13521 can read from a Serial Flash Memory device meeting the following requirements.

Table 17-3: Serial Flash Memory Requirements

Parameter	Requirements
Speed	20Mhz and above
FAST READ Command Support	Must be supported by serial flash
Memory Size	150K bytes (minimum)

Note
For an overview of the Serial Flash Memory contents, see 9.2, “Serial Flash Memory Contents” on page 55.

17.3.1 Serial Flash Memory Connection Example

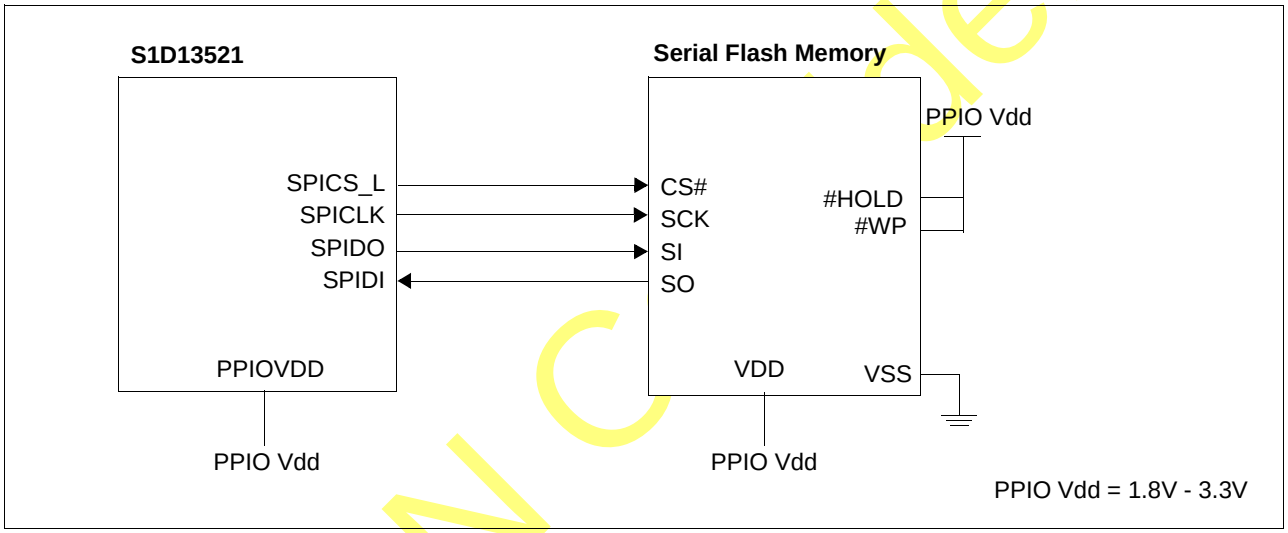


Figure 17-4: Example Serial Flash Memory Connection

17.3.2 Serial Flash Memory Operation Timing

S1D13521 SPI controller provides low level operations only. Each operation trigger is a single byte Read/Write transfer on the SPI interface. Software must control the behavior of CS#. For SPI programming examples, refer to 13.2, “Flash Memory Accesses using SPI Interface Registers” on page 118.

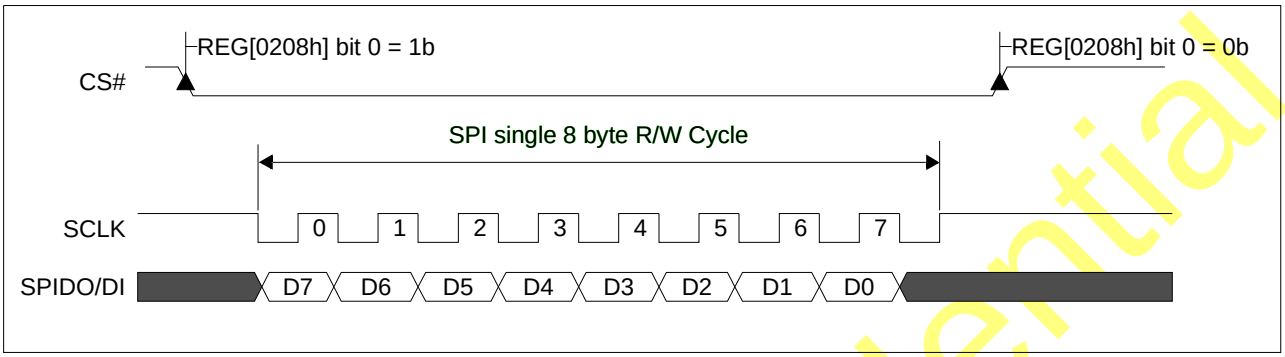


Figure 17-5: SPI Flash Memory Operation Timing

17.4 SDRAM

The S1D13521 supports SDRAM meeting the following requirements.

Table 17-4: SDRAM Requirements

Parameter	Requirements
Speed	100Mhz and above
Width	16-bit or 32-bit
Column Width	256, 512, 1K or 2K
Banks	4 Banks
Voltage	1.8V, 3.0V, 3.3V
Timing (RAS, CAS, RCD)	2 or 3 clocks
Mobile SDRAM	Optional EMR support
Self Refresh	Must be supported
SDRAM Size Requirement	Pixel Width x Pixel Height x 3 = Bytes required

17.4.1 SDRAM Size Requirements

The SDRAM size required for a specific implementation is determined based on the display size and is independent of the selected waveform bit depth.

The S1D13521 SDRAM space is comprised of the Update Buffer, which requires two bytes for each pixel, and the Image Buffer, which requires one byte for each pixel. Therefore, the following calculation should be used to determine the correct SDRAM size:

Minimum SDRAM size = display width in pixels x display height in lines x 3 bytes per pixel

For example, the minimum SDRAM requirement for a 6 inch, 800x600 AMEPD is calculated as follows.

Minimum SDRAM size = display width in pixels x display height in lines x 3 bytes per pixel
= 800 x 600 x 3 bytes
= 1,440,000 bytes

17.4.2 SDRAM Connection Example

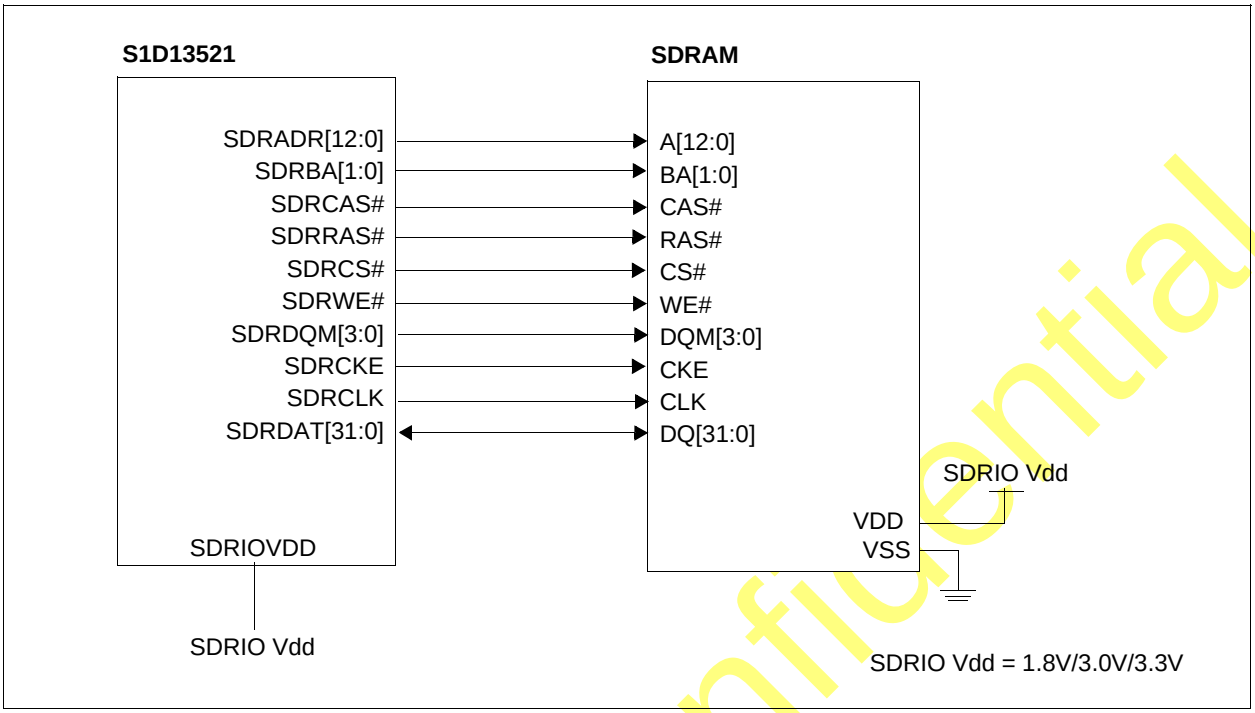


Figure 17-6: Example SDRAM Connection

Note
SDRDAT[31:0] are normally driven low when not actively transferring data, therefore pull-up or pull-down resistors are not necessary.

17.4.3 SDRAM Operation Timing

SDRAM Initialization

SDRAM Initialization is started with a SDRAM Initialization Trigger. The S1D13521 can be configured to wait until the SDRAM clock is stable (100us or 200us), before asserting the precharge all command. This is followed by the 8 Auto Refresh Command, and then the Load Mode Register command is asserted. For Mobile SDRAM, the optional Extended Load Mode Register command is asserted 4 clocks later. The SDRAM clock is completely shut off 3 clocks after CKE is deasserted and the Initialize Done Status/Interrupt is asserted 3 clocks later.

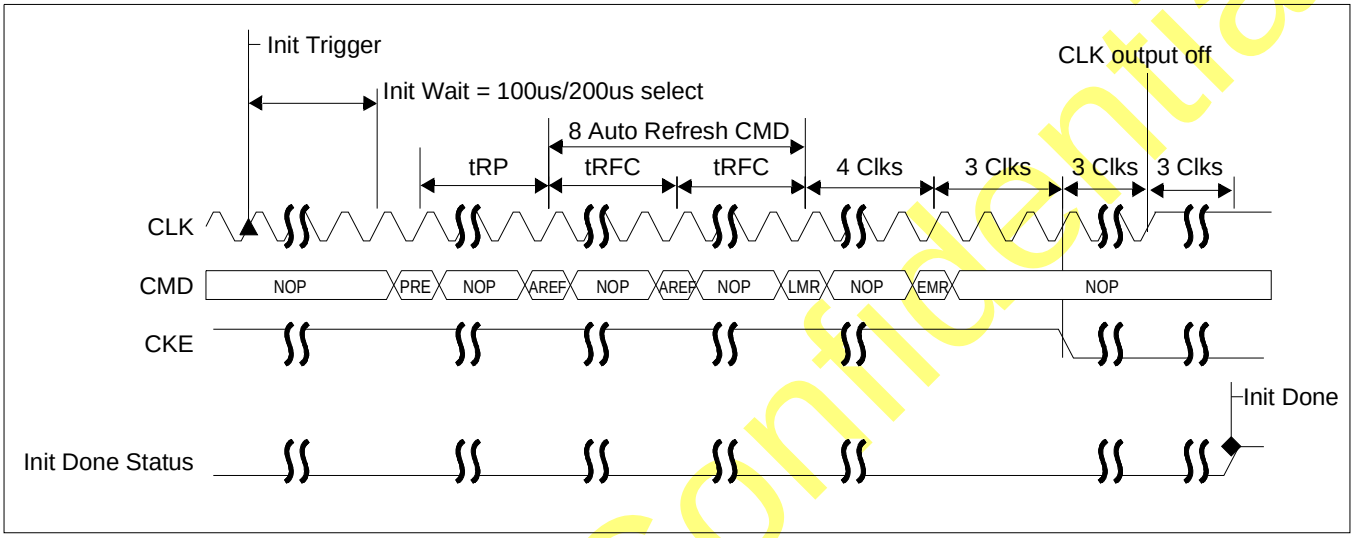


Figure 17-7: SDRAM Initialization Operation Timing

SDRAM Self Refresh

When the Enter Self Refresh sequence is started, a Precharge all banks is asserted. After the tRP timing is met, a Self Refresh Command is asserted with CKE “LOW” to enter self refresh. CLK will be turned off after a 2 clock pulse. When the Exit Self Refresh sequence is started, 1 clock pulse is available before CKE is asserted high again. A minimum of tRFC must pass before any Row Active commands are allowed.

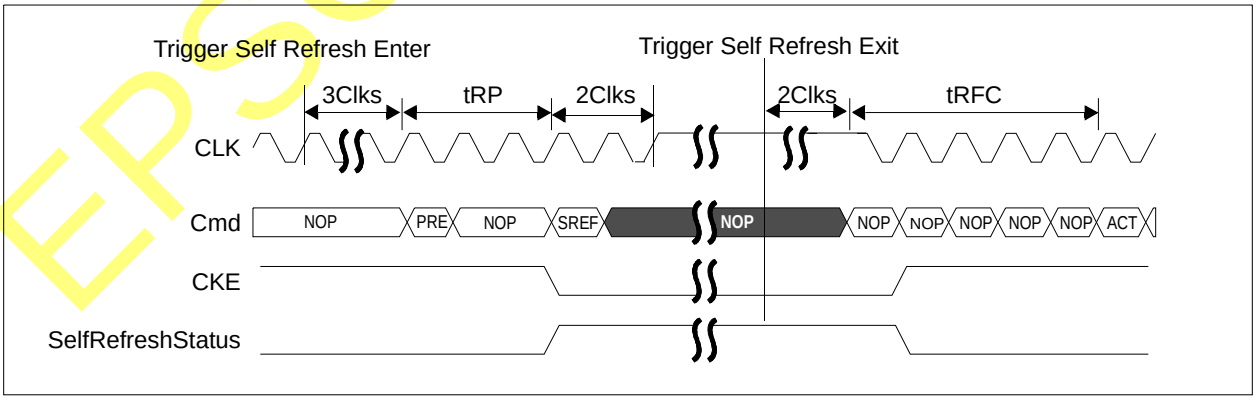


Figure 17-8: SDRAM Self Refresh Timing

SDRAM Auto Refresh

SDRAM Auto Refresh is requested using the refresh clock derived from the divided external input clock CLKI (see REG[0106h]). Typically, an Auto Refresh starts with a Precharge command, followed by an Auto Refresh request.

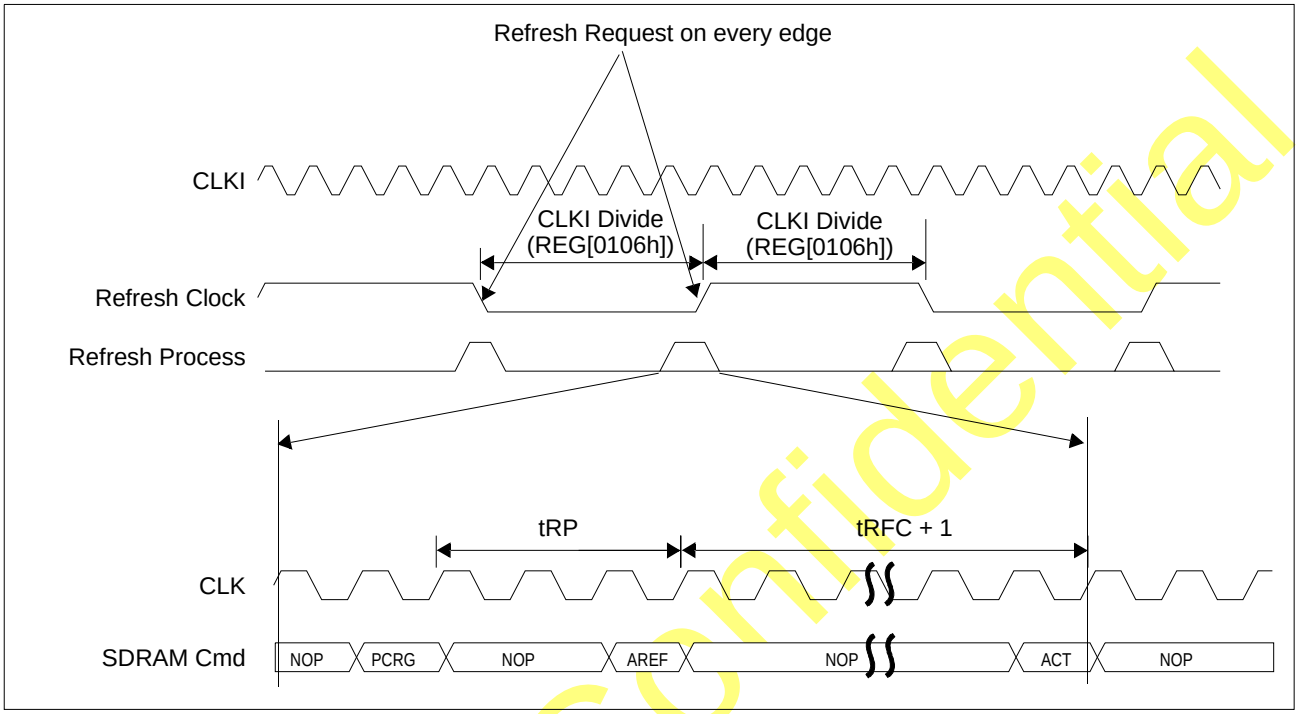


Figure 17-9: Auto Refresh Command Timing

SDRAM Read

The SDRAM read process starts with a Row Active Command. tRCD timing is waited for before any Column Read operation takes place. The Read Data is expected to be available on the DQ bus 2 or 3 clocks later, depending on the tCL setting. An opened Row must meet the minimum Row Open Time (tRAS) before a manual Precharge command is asserted. The Precharge command is followed by the tRP minimum timing before a new Row Open command is allowed.

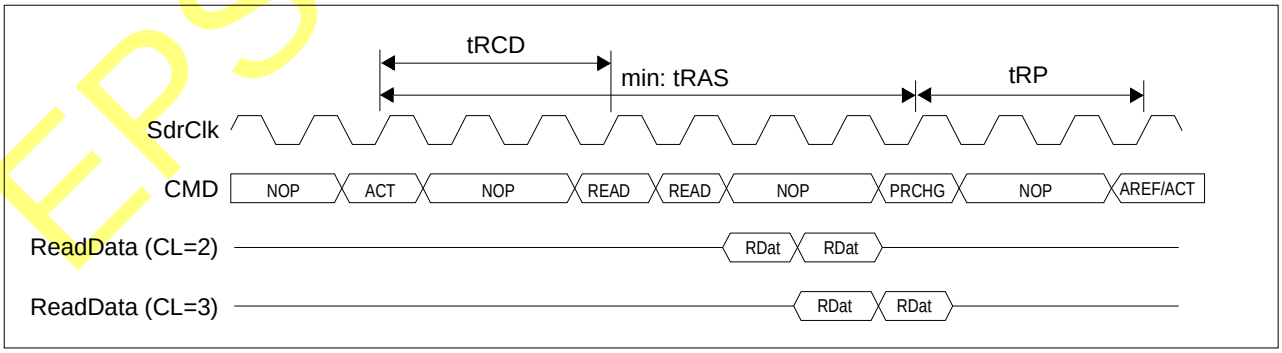


Figure 17-10: SDRAM Read Timing

SDRAM Write

SDRAM Write process starts with a Row Active Command. tRCD timing is waited for before any Column Write + Data operation takes place. The Write Data is presented on the bus at the same time as the WRITE Command. An opened Row must meet the minimum Row Open Time (tRAS) before a manual Precharge command is asserted. The Precharge command is followed by the tRP minimum timing before a new Row Open command is allowed.

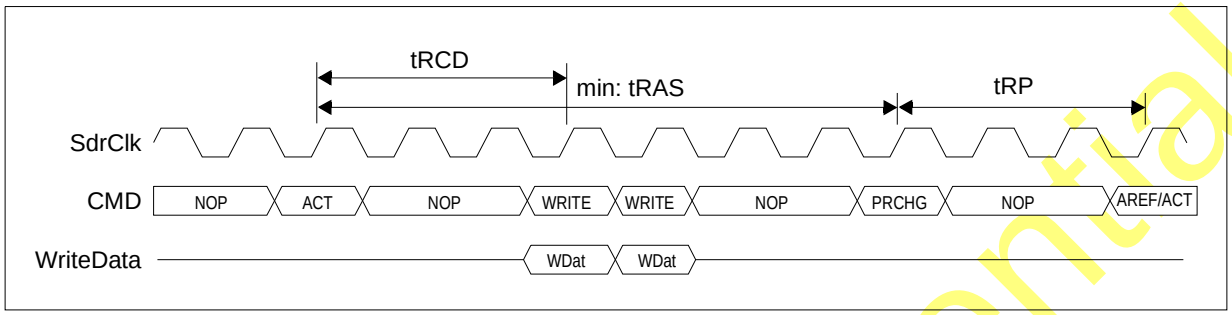


Figure 17-11: SDRAM Write Timing

SDRAM Active Power Down

SDRAM Active Power Down is enabled whenever the SDRAM controller is idling. Active power down will commence on the last command asserted (LCMD, i.e. Precharge all banks and Auto Refresh Command). The minimum timing requirements depend on the last command. For Precharge all banks, tRP must be met. For Auto Refresh Command, tRFC must be met.

Active Power Down will never last longer than an Auto Refresh Cycle. When an Auto Refresh occurs, the SDRAM controller will briefly exit Active Power Down to perform the Auto Refresh Command. Once the Auto Refresh Command is complete and the SDRAM controller is idle again, it will return to the Active Power Down state.

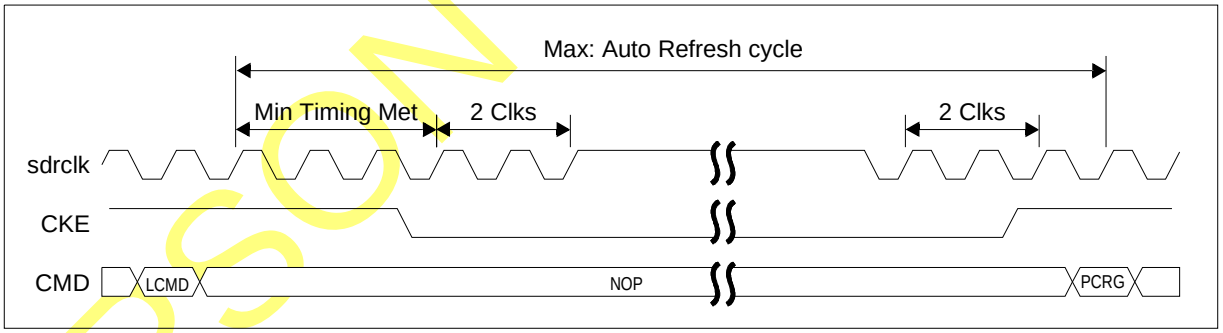


Figure 17-12: SDRAM Active Power Down Timing

17.5 3-Wire Power Management

The S1D13521 supports power management using a 3-wire Active Matrix Power Management IC. The power management device must meet the following requirements.

Table 17-5: 3-Wire Power Management Requirements

Parameter	Requirements
Interface	3 - wire type (Chip Select, DATA and Clock)
Interface Speed	10Mhz and above
(VNEGS, VPOSS) Programming Register Address	0x31
(VEES, VCCS) Programming Register Address	0x32
(VCOMS) Programming Register Address	0x22
(DUMMY) Programming Register Address	0x24
Temperature Retrieval Register Address	0x11

17.5.1 3-Wire Power Management Connection Example

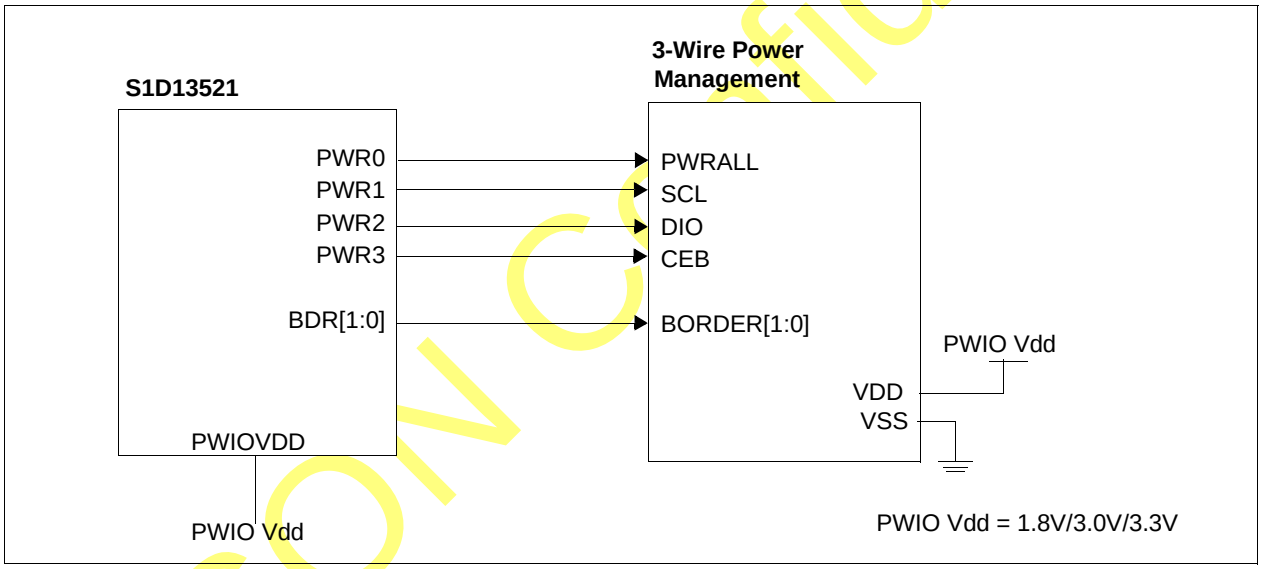


Figure 17-13: Example 3-Wire Power Management Connection

17.5.2 3-Wire Power Management Operation Timing

A single 3-wire byte Read/Write always begins with a two bit start sequence. The Address Byte is next, followed by the data byte to be written or read.

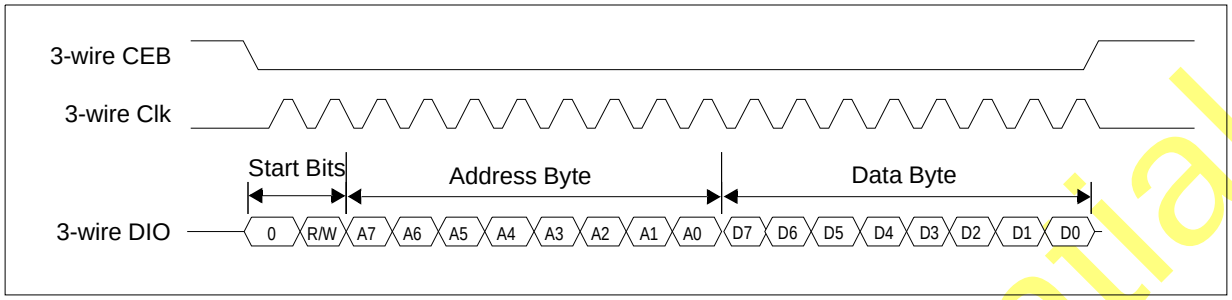


Figure 17-14: 3-Wire Operation Timing

Chapter 18 OSC Clock Timing Requirements

The S1D13521 has an internal oscillator which has specific startup time requirements. When using the internal oscillator (CNF2=1), these timing requirements must be observed or the Command Interface hardware will not be able to perform a normal boot-up initialization sequence which will result in a system failure for the S1D13521.

A typical oscillator requires a large amount of startup time before it can provide a stable peak-to-peak clock. During this startup time the analog circuit does not provide the correct peak-to-peak operating voltage and the internal digital logic is unable to recognize the correct clock transitions. The following figure shows this situation.

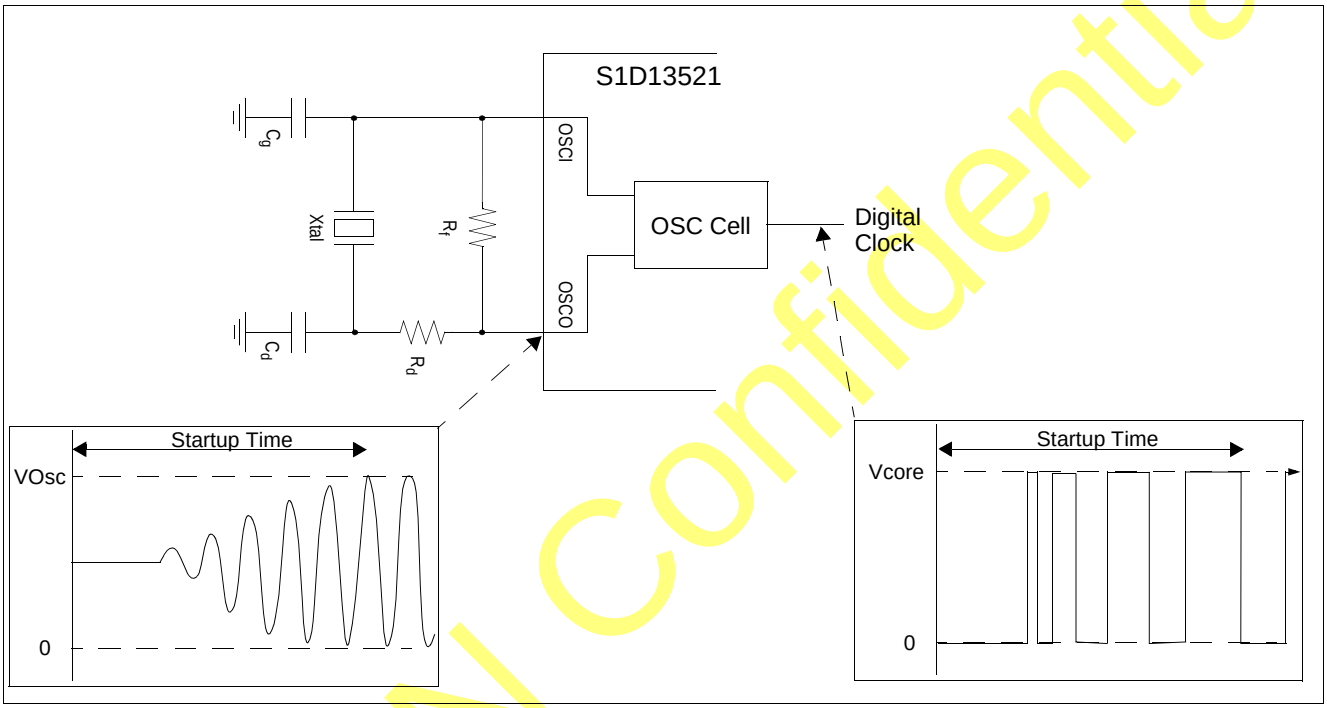


Figure 18-1: Oscillator Clock Capture on Analog and Digital Side

Note
For details on the recommended OSC circuit, see 17.1, “OSC Circuit” on page 133.

18.1 Timing Requirements For Reset

The Command Interface automatically accesses the serial flash interface when Reset is deasserted. Therefore, the S1D13521 must have a stable clock before Reset is deasserted. The Reset timing requirements are different depending on the input clock source.

18.1.1 Input Clock From OSCI/OSCO

When the input clock is from OSCI/OSCO (CNF2=1), the following reset timing is required.

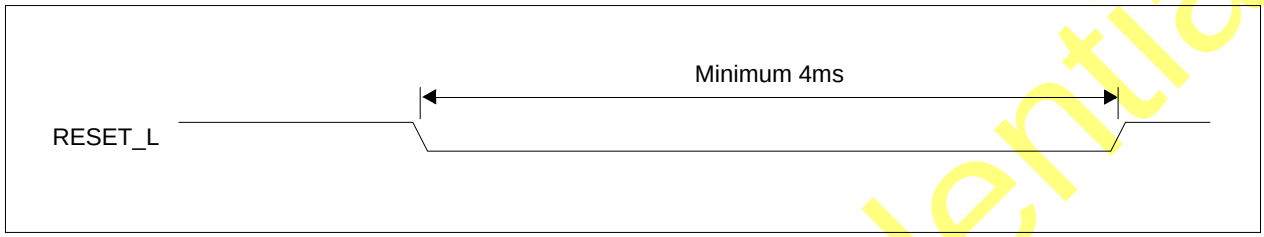


Figure 18-2: Reset Timing Requirement for Input Clock From Oscillator

A 25MHz crystal with a 30pf capacitor (see 17.1, “OSC Circuit” on page 133) requires a minimum of 4ms before the clock becomes stable. For this case, the following programming flow is recommended.

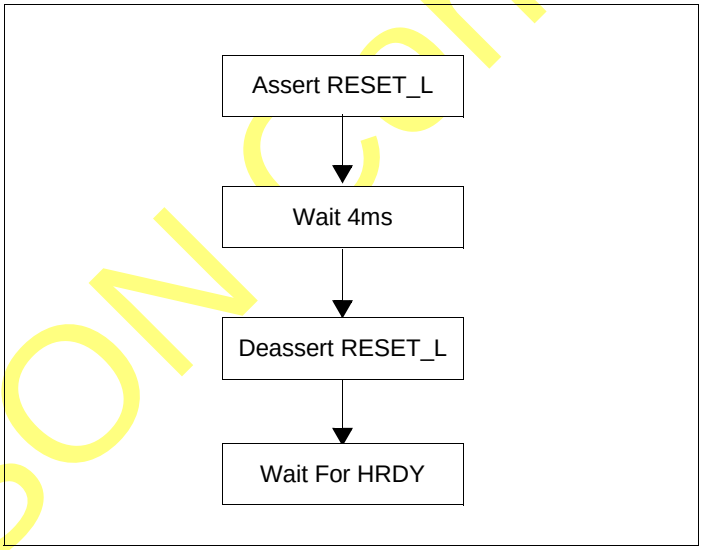


Figure 18-3: Reset Timing Requirement Programming Flow for Input Clock From Oscillator

18.1.2 Input Clock From CLKI

When the input clock is from CLKI (CNF2=0), the following reset timing is required.

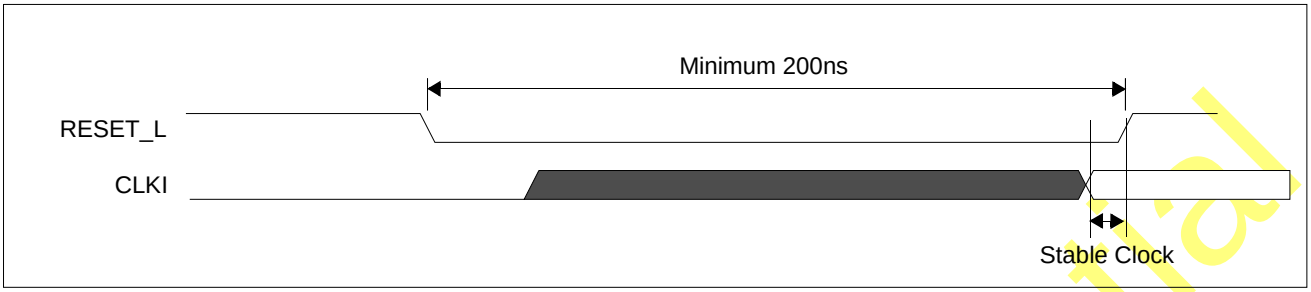


Figure 18-4: Reset Timing Requirement for Input Clock From CLKI

Note
The stable clock must have the correct Duty cycle and Peak-to-Peak voltage.

For this case, the following programming flow is recommended.

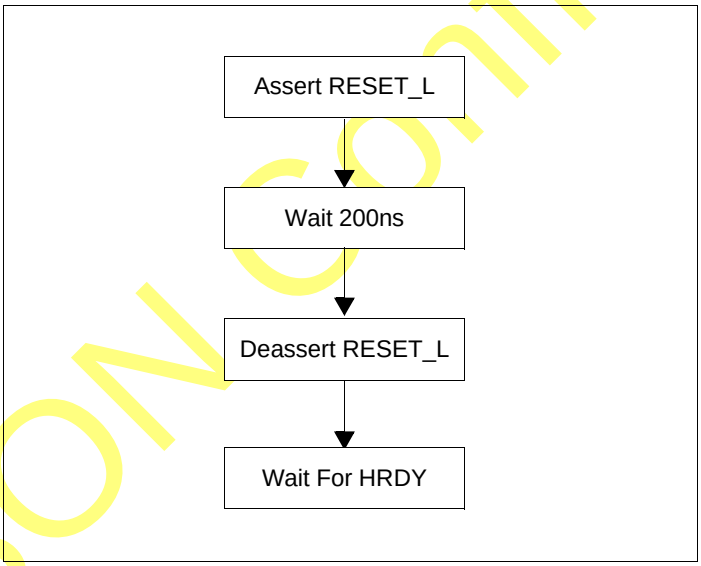


Figure 18-5: Reset Timing Requirement Programming Flow for Input Clock From CLKI

18.2 Timing Requirements For Exiting From Sleep Mode

When the S1D13521 exits sleep mode, it requires a stable clock before any new cycles can be executed. The procedure used to exit sleep mode varies depending on the input clock source.

18.2.1 Input Clock from OSCI/OSCO

When the input clock is from OSCI/OSCO (CNF2=1), the following timing is required.

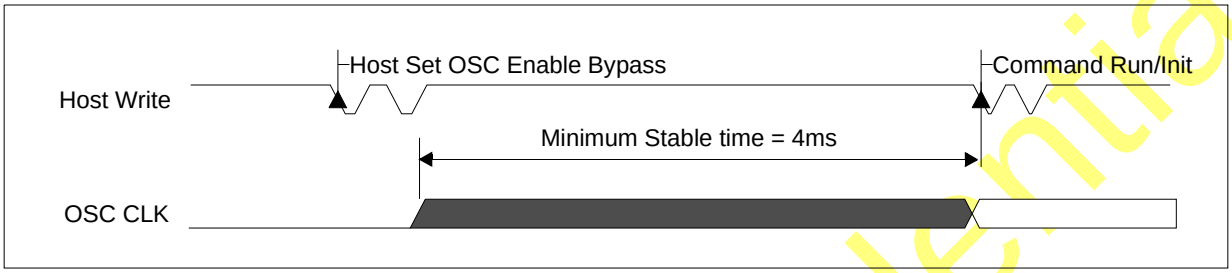


Figure 18-6: Exiting Sleep Timing Requirement for Input Clock From Oscillator

A 25MHz crystal with a 30pf capacitor (see 17.1, “OSC Circuit” on page 133) requires a minimum of 4ms before the clock becomes stable. In this case, the following programming flow is recommended.

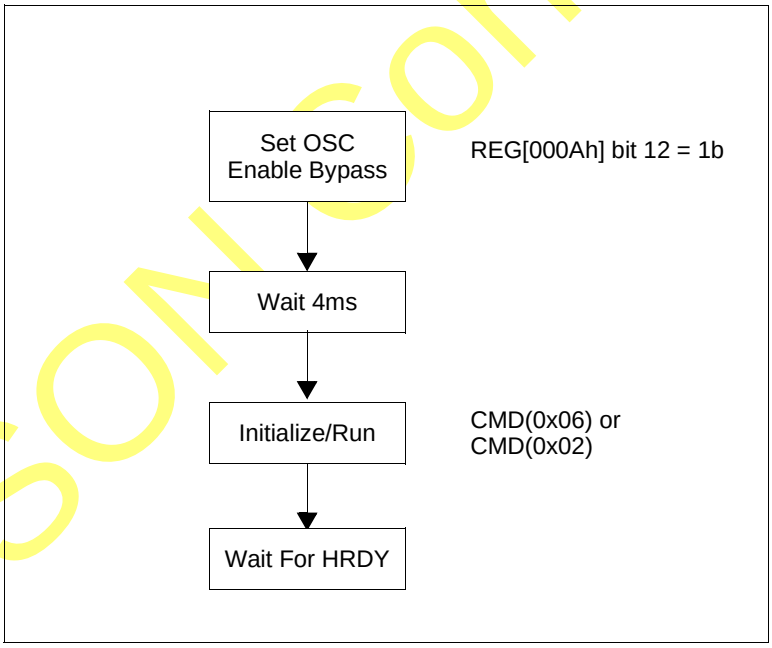


Figure 18-7: Exiting Sleep Programming Flow for Input Clock From Oscillator

18.2.2 Input Clock from CLKI

When the input clock is from CLKI (CNF2=0), the CLKI input must be stable for a least 1 CLK pulse before issuing a Command Run or Command Init sequence.

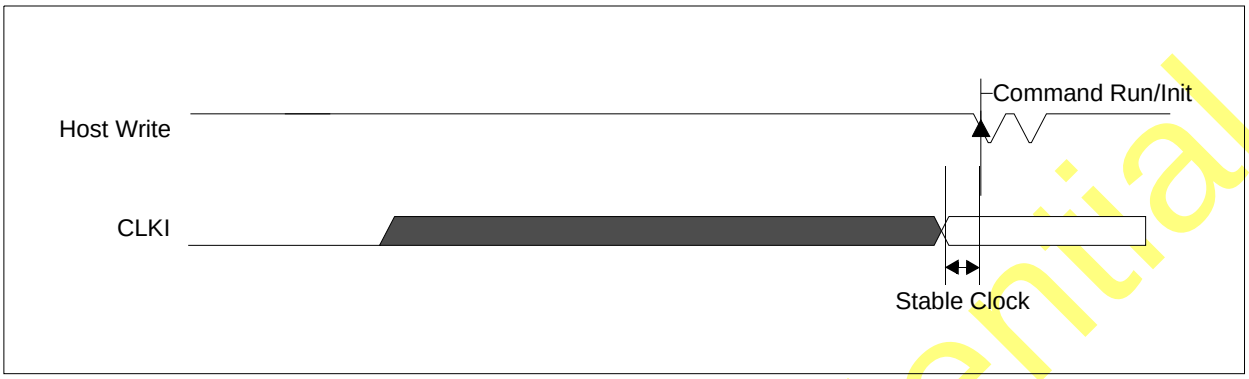


Figure 18-8: Exiting Sleep Timing Requirement for Input Clock From CLKI

In this case, the following programming flow is recommended.

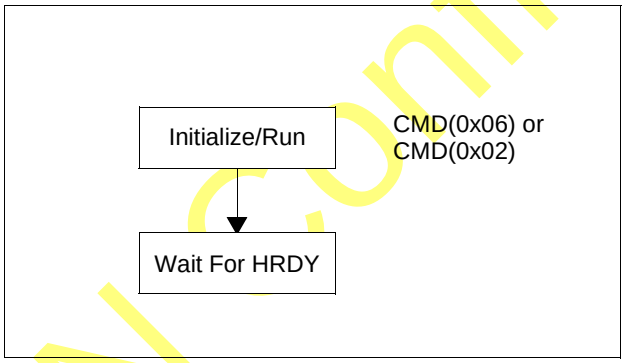


Figure 18-9: Exiting Sleep Programming Flow for Input Clock From CLKI

Chapter 19 Analog Power Supply Considerations

The PLL circuit is an analog circuit which is very sensitive to noise on the input clock waveform or the power supply. Noise on the clock or the supplied power may cause the operation of this circuit to become unstable or increase the jitter.

Due to these noise constraints, it is highly recommended that the power supply traces or the power plane for this circuit be isolated from those of other power supplies. Filtering should also be used to keep the power as clean as possible.

The following are guidelines which, if followed, will result in cleaner power to the PLL circuit. This will result in a cleaner and more stable clock. Even a partial implementation of these guidelines will give results.

19.1 Guidelines for Analog Power Layout

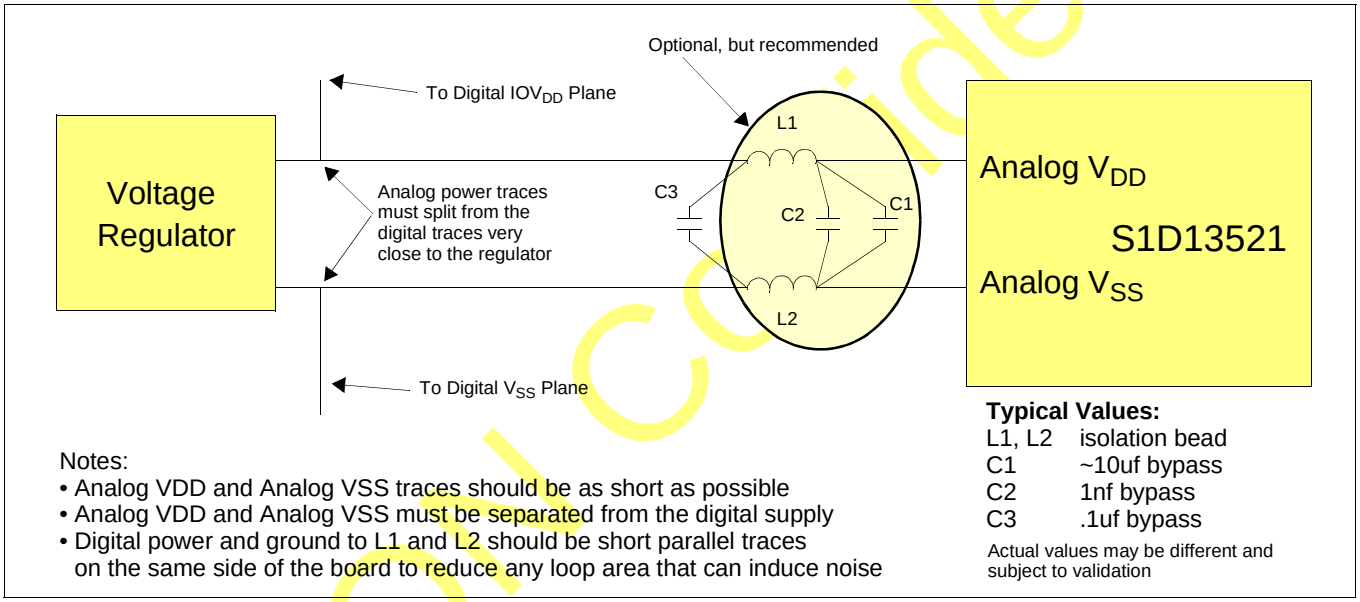


Figure 19-1: Analog Power Layout

- Place the ferrite beads (L1 and L2) parallel to each other with minimal clearance between them. Both bypass caps (C2 and C3) should be as close as possible to the inductors. The traces from C3 to the power planes should be short parallel traces on the same side of the board with just the normal small clearance between them. Any significant loop area here will induce noise. If there is a voltage regulator on the board, try to run these power traces directly to the regulator instead of dropping to the power planes (still follow above rules about parallel traces).
- The analog ground point where bypass cap (C2) connects to the ground isolation inductor (L2) becomes the analog ground central point for a ground star topology. None of the components connect directly to the analog ground pin of the S1D13521 ($PLLV_{SS}$) except for a single short trace from C2 to the $PLLV_{SS}$ pin. The ground side of the large bypass capacitor (C1) should also have a direct connection to the star point.

- The same star topology rules used for analog ground apply to the analog power connection where L2 connects to C2.
- All of the trace lengths should be as short as possible.
- If possible, have all the PLL traces on the same outside layer of the board. The only exception is C1, which can be put on the other side of the board if necessary. C1 does not have to be as close to the analog ground and power star points as the other components.
- If possible, include a partial plane under the PLL area only (area under PLL components and traces). The solid analog plane should be grounded to the C2 (bypass) pad. This plane won't help if it is too large. It is strictly an electrostatic shield against coupling from other layers' signals in the same board area. If such an analog plane is not possible, try to have the layer below the PLL components be a digital power plane instead of a signal layer.
- If possible, keep other board signals from running right next to PLL pin vias on any layer.
- Wherever possible use thick traces, especially with the analog ground and power star connections to either side of C2. Try to make them as wide as the component pads – thin traces are more inductive.

It is likely that manufacturing rules will prohibit routing the ground and power star connections as suggested. For instance, four wide traces converging on a single pad could have reflow problems during assembly because of the thermal effect of all the copper traces around the capacitor pad. One solution might be to have only a single trace connecting to the pad and then have all the other traces connecting to this wide trace a minimum distance away from the pad. Another solution might be to have the traces connect to the pad, but with thermal relief around the pad to break up the copper connection. Ultimately the board must also be manufacturable, so best effort is acceptable.

Chapter 20 Mechanical Data

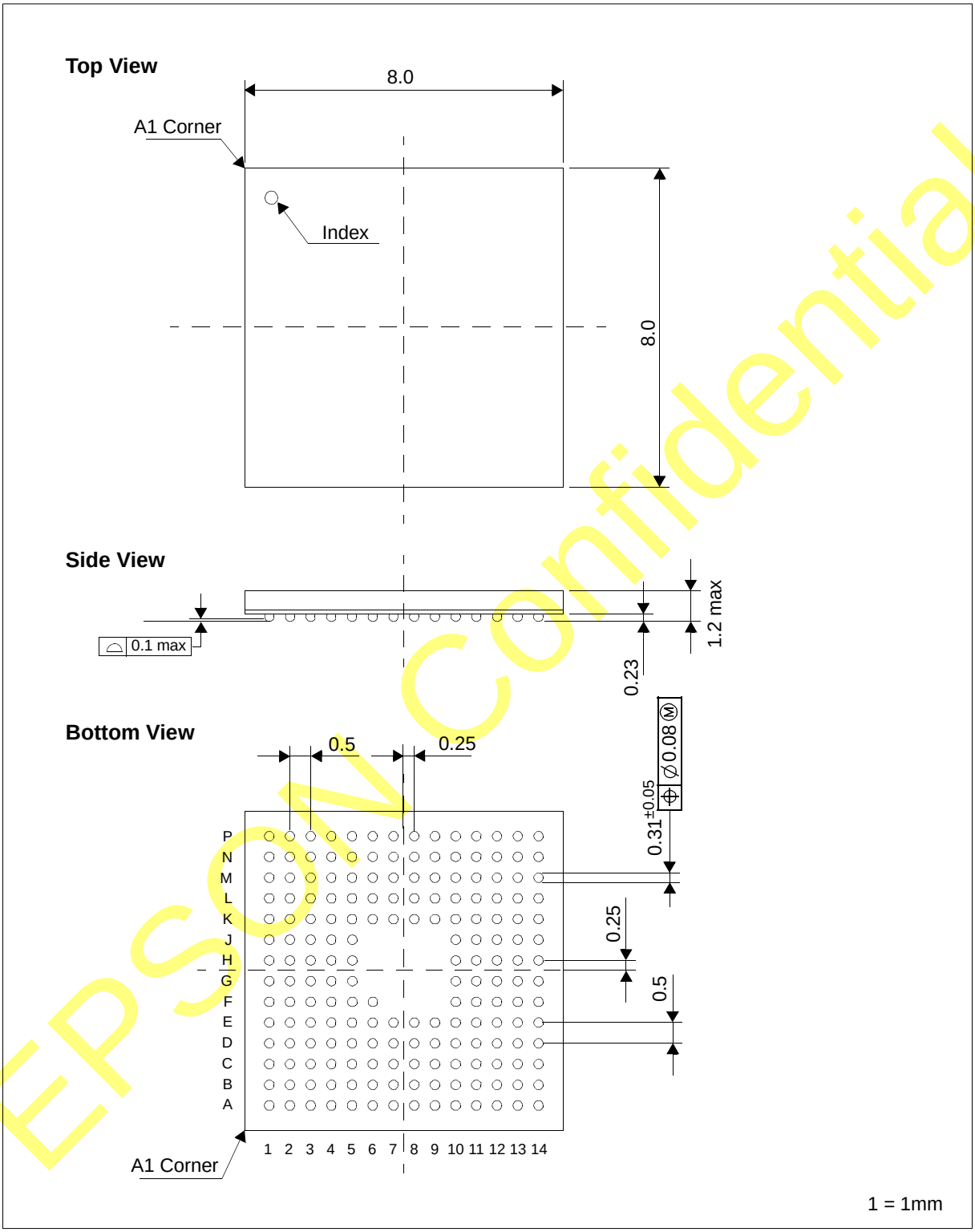
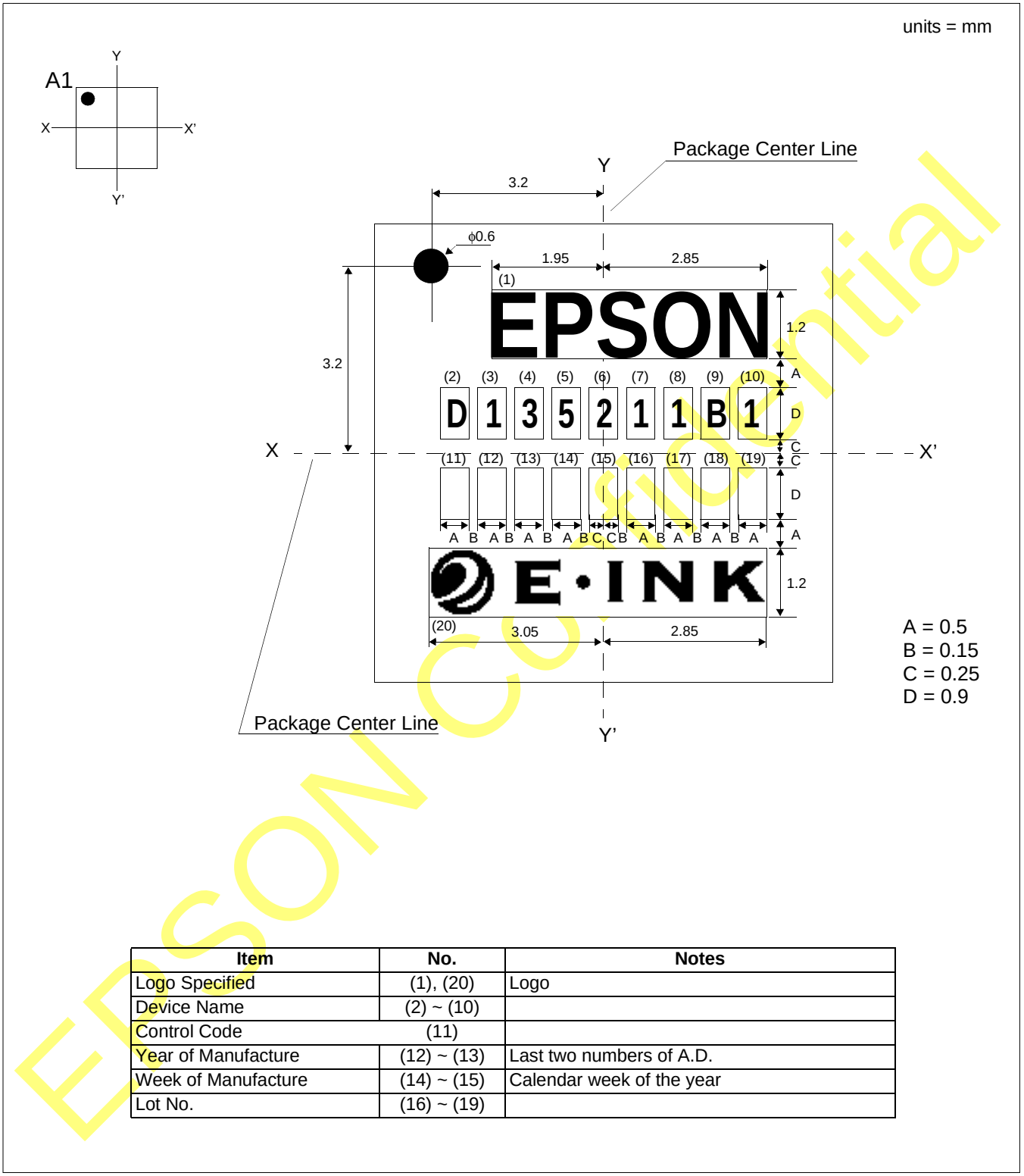


Figure 20-1: PFBGA8UX 181-pin Package



Item	No.	Notes
Logo Specified	(1), (20)	Logo
Device Name	(2) ~ (10)	
Control Code	(11)	
Year of Manufacture	(12) ~ (13)	Last two numbers of A.D.
Week of Manufacture	(14) ~ (15)	Calendar week of the year
Lot No.	(16) ~ (19)	

Figure 20-2: S1D13521 PFBGA8UX 181-pin Package Marking

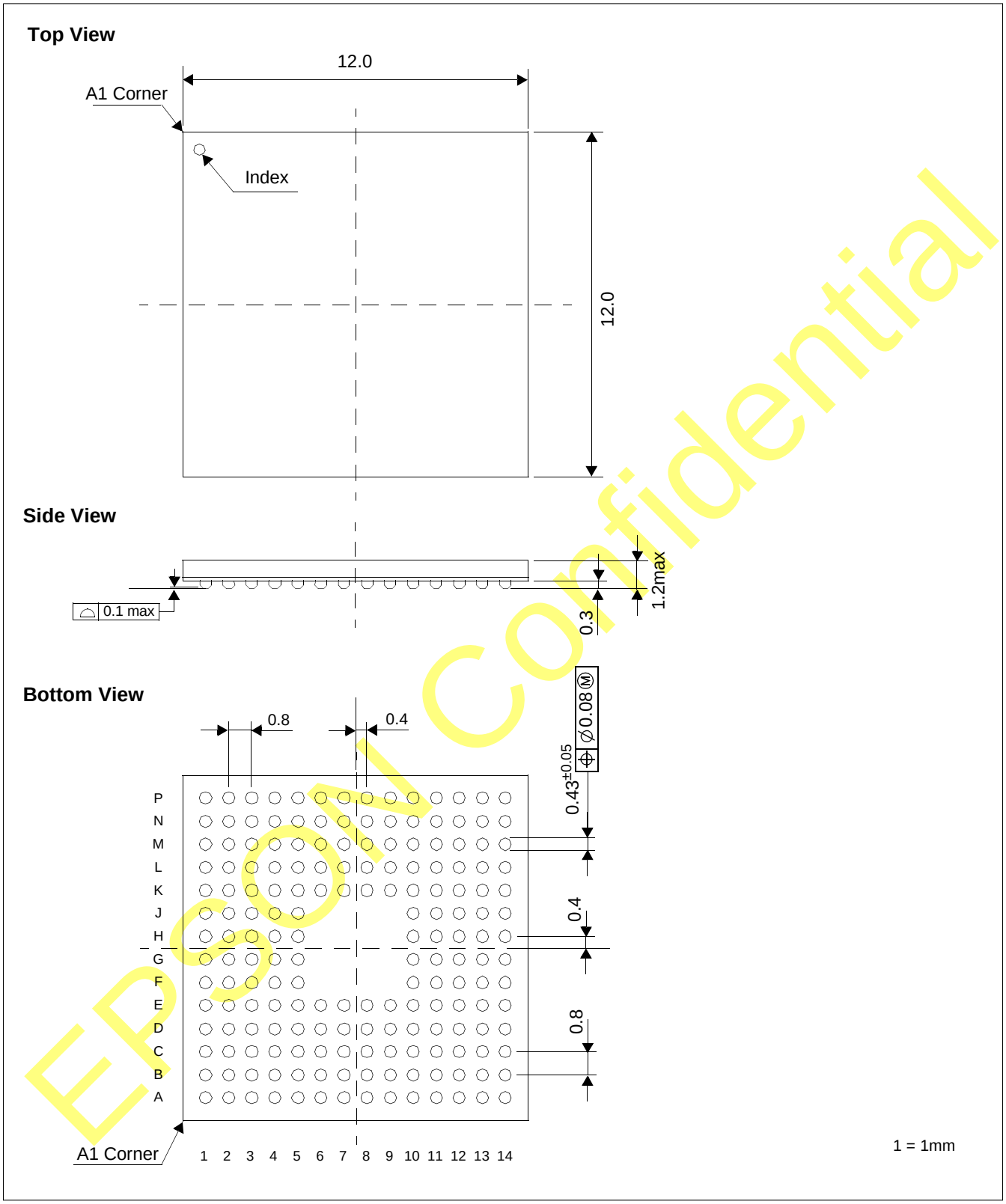
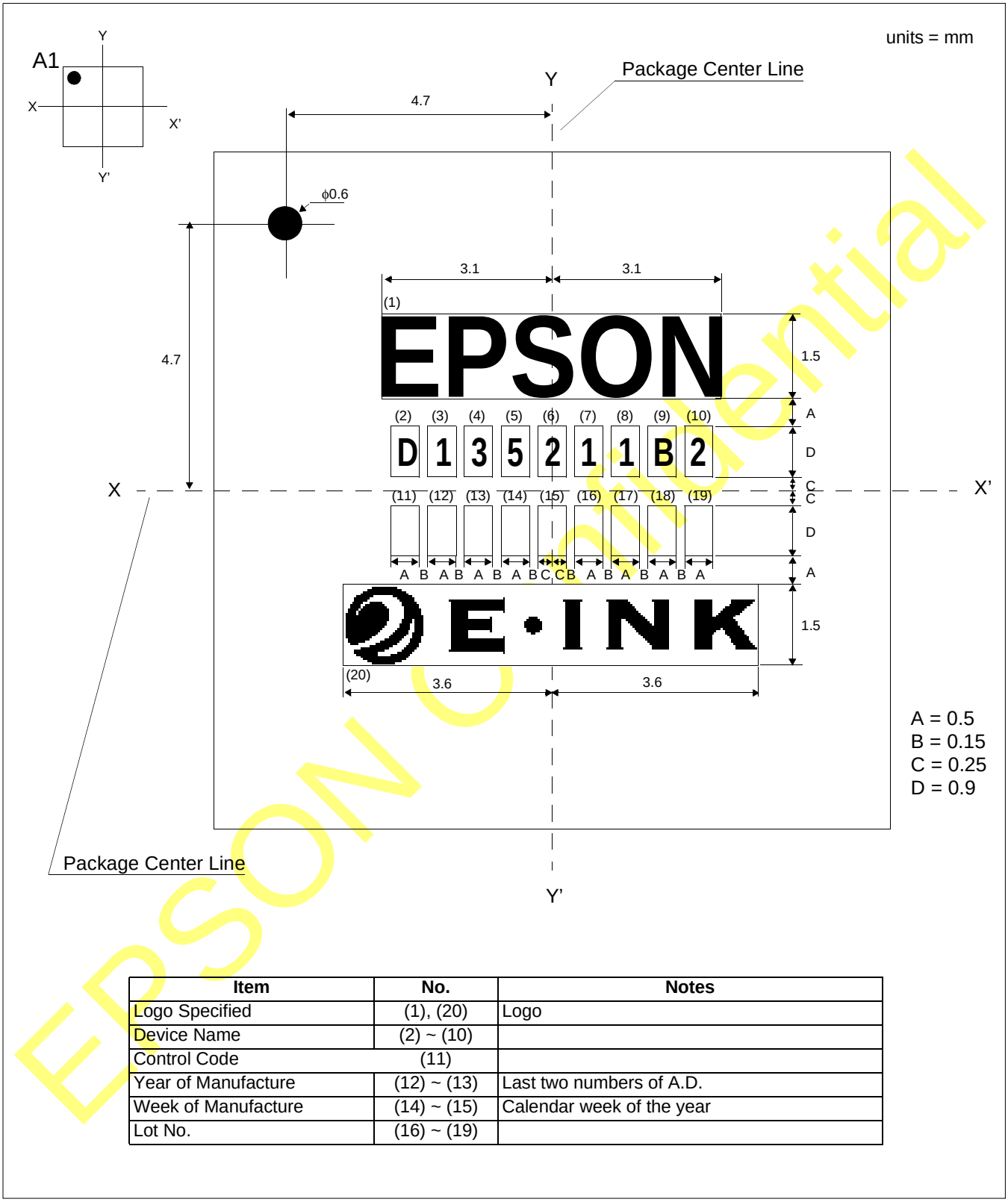


Figure 20-3: PFBGA12UX 180-pin Package



Item	No.	Notes
Logo Specified	(1), (20)	Logo
Device Name	(2) ~ (10)	
Control Code	(11)	
Year of Manufacture	(12) ~ (13)	Last two numbers of A.D.
Week of Manufacture	(14) ~ (15)	Calendar week of the year
Lot No.	(16) ~ (19)	

Figure 20-4: S1D13521 PFBGA12UX 180-pin Package Marking

20.1 Thermal Details

The thermal details for the PFBGA8UX 181-pin package are as follows:

θja : 31°C / W (max ±10°C / W)

The thermal details for the PFBGA12UX 180-pin package are as follows:

θja : 24°C / W (max ±10°C / W)

Chapter 21 References

The following documents contain additional information related to the S1D13521. Document numbers are listed in parenthesis after the document name. All documents can be found at the Epson Research and Development Website at **www.erd.epson.com**.

- S1D13521 Product Brief (X88A-C-001-xx)

Appendix A Registers

This section discusses how and where to access the S1D13521 registers. It also provides detailed information about the layout and usage of each register.

A.1 Register Access

The S1D13521 registers are 16-bit wide. They can be accessed using the Command Interface

A.1.1 Register Access using Command Interface

Registers may be accessed using the command interface with the following sequences.

For single 16-bit register reads:

Table 21-1: Register Read Sequence

Tx Count	16-bit Indirect Host
0	Write Code[15:0] <= 0x0010
1	Write Register Address[15:0]
2	Read

For single 16-bit register writes:

Table 21-2: Register Write Sequence

Tx Count	16-bit Indirect Host
0	Write Code[15:0] <= 0x0011
1	Write Register Address[15:0]
2	Write

Note
Only single register accesses are supported (i.e. register address is not auto incremented to the next register address).

Table 21-3: Register Mapping

Address Range	Register Type	Description
0000h to 000Ah	Asynchronous	System Configuration Registers
0010h to 001Ah	Asynchronous	Clock Configuration Registers
0020h	Asynchronous	Component Configuration
0100h to 010Ch	Synchronous	Memory Controller Configuration
0140h to 0158h	Synchronous	Host Interface Memory Access Configuration
0200h to 0208h	Synchronous	SPI Flash Memory Interface
0210h to 0216h	Synchronous	I2C Thermal Sensor Interface Registers
0220h to 0226h	Synchronous	3-Wire Chip Interface Registers
0230h to 0238h	Synchronous	Power Pin Control Configuration Registers
0240h to 0244h	Synchronous	Interrupt Configuration Registers
0250h to 0256h	Synchronous	GPIO Control Registers
0290h to 02A2h	Synchronous	Command RAM Controller Registers
0300h to 035Eh	Synchronous	Display Engine Registers
0360h to 036Eh	Synchronous	Auto Waveform Mode Configuration Registers

A.2 Register Set

The S1D13521 registers are listed in the following table.

Table 21-4: S1D13521 Register Set

Table 21-4: S1D13521 Register Set (Continued)

Register	Pg	Register	Pg
REG[0290h] Command RAM Controller Configuration Register	204	REG[0292h] Command RAM Controller Address Register	204
REG[0294h] Command RAM Controller Access Port Register	204	REG[02A0h] through REG[02A2h] are Reserved	
Display Engine: Display Timing Configuration			
REG[0300h] Frame Data Length Register	205	REG[0302h] Frame Sync Length Register	205
REG[0304h] Frame Begin/End Length Register	205	REG[0306h] Line Data Length Register	206
REG[0308h] Line Sync Length Register	206	REG[030Ah] Line Begin/End Length Register	207
Display Engine: Driver Configurations			
REG[030Ch] Source Driver Configuration Register	208	REG[030Eh] Gate Driver Configuration Register	210
Display Engine: Memory Region Configuration Registers			
REG[0310h] Image Buffer Start Address Register 0	212	REG[0312h] Image Buffer Start Address Register 1	212
REG[0314h] Update Buffer Start Address Register 0	212	REG[0316h] Update Buffer Start Address Register 1	212
Display Engine: Component Control			
REG[0320h] Temperature Device Select Register	213	REG[0322h] Temperature Value Register	213
REG[0324h] is Reserved	213	REG[0326h] Border Configuration Register	213
REG[0328h] is Reserved	214	REG[032Ah] Power Control Configuration Register	214
REG[032Ch] General Configuration Register	215	REG[032Eh] LUT Mask Register	215
Display Engine: Control/Trigger Registers			
REG[0330h] Update Buffer Configuration Register	216	REG[0332h] Update Buffer Pixel Set Value Register	217
REG[0334h] Display Engine Control/Trigger Register	217		
Display Engine: Update Buffer Status Registers			
REG[0336h] Lookup Table Status Register	220	REG[0338h] Display Engine Busy Status Register	220
Display Engine: Interrupt Registers			
REG[033Ah] Display Engine Interrupt Raw Status Register	223	REG[033Ch] Display Engine Interrupt Masked Status Register	226
REG[033Eh] Display Engine Interrupt Enable Register	229		
Display Engine: Partial Update Configuration Register			
REG[0340h] Area Update Pixel Rectangular X-Start Register	232	REG[0342h] Area Update Pixel Rectangular Y-Start Register	233
REG[0344h] Area Update Pixel Rectangular X-End / Horizontal Size Register	234	REG[0346h] Area Update Pixel Rectangular Y-End / Vertical Size Register	235
REG[0348h] Host Pixel Rectangular X-Start Register	236	REG[034Ah] Host Pixel Rectangular Y-Start Register	236
REG[034Ch] Host Pixel Rectangular X-End Register	237	REG[034Eh] Host Pixel Rectangular Y-End Register	237
Display Engine: Serial Flash Waveform Registers			
REG[0350h] Waveform Header Serial Flash Address Register 0	238	REG[0352h] Waveform Header Serial Flash Address Register 1	238
REG[0354h] through REG[035Eh] are Reserved			
Auto Waveform Mode Configuration Registers			
REG[0360h] Auto Waveform Mode Compare 0 Configuration Register 240		REG[0362h] Auto Waveform Mode Compare 0 Current/Next Register 240	
REG[0364h] Auto Waveform Mode Compare 1 Configuration Register 241		REG[0366h] Auto Waveform Mode Compare 1 Current/Next Register 241	
REG[0368h] Auto Waveform Mode Compare 2 Configuration Register 242		REG[036Ah] Auto Waveform Mode Compare 2 Current/Next Register 242	
REG[036Ch] Auto Waveform Mode Compare 3 Configuration Register 243		REG[036Eh] is Reserved	

A.3 Register Descriptions

A.3.1 System Configuration Registers

REG[0000h] Revision Code Register
Default = 0000h — Read Only

15	14	13	12	11	10	9	8
Revision Code bits 15-8							
7	6	5	4	3	2	1	0
These bits always return 0000_0000b							

bits 7-0 These bits always return 0000_0000b.

bits 15-8 Revision Code bits [7:0] (Read Only)
These bits indicate the revision code.
The revision code for the S1D13521B01 is 01h.

REG[0002h] Product Code Register
Default = 0047h — Read Only

15	14	13	12	11	10	9	8
Product Code bits 15-8							
7	6	5	4	3	2	1	0
Product Code bits 7-0							

bits 15-0 Product Code bits [15:0] (Read Only)
These bits indicate the product code.
The product code for the S1D13521 is 0047h.

REG[0004h] Config Pin Read Value Register
Default = 000Xh — Read Only

15	14	13	12	11	10	9	8
n/a							
7	6	5	4	3	2	1	0
n/a				CNF[3:0] Status			

bits 3-0 CNF[3:0] Status (Read Only)
These bits return the status of the configuration pins CNF[3:0]. For a functional description of each CNF[3:0] pin, see 4.2.10, “Miscellaneous” on page 22.

REG[0006h] Power Save Mode Register
Default = 0001h — Read/Write

15	14	13	12	11	10	9	8
n/a							

7	6	5	4	3	2	1	0
n/a							Power Save Mode Enable

bit 0 Power Save Mode Enable

This bit controls power save mode.
When this bit = 0b, power save mode is disabled.
When this bit = 1b, power save mode is enabled and all clocks are gated off. (default)

This bit in combination with the PLL Power Down (REG[0016h] bit 1) and PLL Bypass (REG[0016h] bit 0) bits, define the different power states of the S1D13521. The following table summarizes the possible states of the S1D13521.

Table 21-5: S1D13521 Power States Summary

Power State	Power Save Mode Enable (REG[0006h] bit 0)	PLL Power Down (REG[0016h] bit 1)	PLL Bypass (REG[0016h] bit 0)
OFF	1b	1b	1b
SLEEP	1b	1b	1b
STANDBY (PLL) (See Note)	1b	0b	0b
RUN (PLL)	0b	0b	0b
RUN (CLKI)	0b	1b	1b

Note
When STANDBY (PLL) is selected, all internal clocks are gated off but the PLL remains running. This is done to avoid waiting for the PLL to become stable (PLL lock time) before returning to the RUN (PLL) state. There is no STANDBY (CLKI) state.

REG[0008h] Software Reset Register
Default = not applicable — Write Only

15	14	13	12	11	10	9	8
Software Reset bits 15-8							

7	6	5	4	3	2	1	0
Software Reset bits 7-0							

bits 15-0 Software Reset bits [15:0] (Write Only)

Writing any value to this register performs a software reset of the S1D13521 which sets all registers to their default states and all pins to their RESET# states.

REG[000Ah] System Status Register
Default = 0000h Read/Write

3-Wire Busy Status (RO)	Power Management Busy Status (RO)	n/a	OSC Enable Bypass	Power Save Status bits 1-0		SDRAM Self Refresh Mode Status (RO)	Power Pin Sequence Status (RO)
15	14	13	12	11	10	9	8
I2C Busy Status (RO)	SPI Busy Status (RO)	Host Interface Busy Status (RO)	SDRAM Controller Busy Status (RO)	Host Memory Access Busy Status (RO)	Display Engine Busy Status (RO)	SDRAM Initialized (RO)	PLL Lock (RO)
7	6	5	4	3	2	1	0

bit 15 3-Wire Busy Status (Read Only)
This bit indicates the status for 3-Wire.
When this bit = 0b, 3-Wire is not busy.
When this bit = 1b, 3-Wire is busy.

bit 14 Power Management Busy Status (Read Only)
This bit indicates the status of the Power Management logic.
When this bit = 0b, the Power Management logic is not busy.
When this bit = 1b, the Power Management logic is busy.

bit 12 OSC Enable Bypass
This bit determines whether the OSC is controlled by internal logic.
When this bit = 0b, the OSC is controlled by internal logic.
When this bit = 1b, the OSC is always enabled.

bits 11-10 Power Save Status bits [1:0]
These bits indicate the power save status of the S1D13521.

Table 21-6 : Power Save Status

REG[000Ah] bits 11-10	Power Save Status
00b	Un-initialized System
01b	Run Mode
10b	Standby Mode
11b	Sleep Mode

bit 9 SDRAM Self Refresh Mode Status (Read Only)
This bit indicates whether the SDRAM controller is in self refresh mode. SDRAM self refresh mode is controlled using the SDRAM Enter Self Refresh Trigger bit (REG[0104h] bit 0) and the SDRAM Exit Self Refresh Trigger bit (REG[0104h] bit 1).
When this bit = 0b, the SDRAM controller is not in self refresh mode.
When this bit = 1b, the SDRAM controller is in self refresh mode.

Note
The memory must not be accessed while the SDRAM is in self refresh mode. To read or write to memory, self refresh mode must be exited, REG[0104h] bit 1 = 1b.

bit 8 Power Pin Sequence Status (Read Only)
This bit provides the status of the pin sequence. For further information, see 6.6, “Power Pin Interface” on page 48.
When this bit = 0b, it is currently in a power off state. (default)
When this bit = 1b, it is currently in a power on state.

bit 7 I2C Busy Status (Read Only)
This bit indicates whether the I2C interface is busy.
When this bit = 0b, the I2C interface is idle (not busy).
When this bit = 1b, the I2C interface is busy.

bit 6 SPI Busy Status (Read Only)
This bit indicates whether the SPI interface is busy.
When this bit = 0b, the SPI interface is idle (not busy).
When this bit = 1b, the SPI interface is busy.

bit 5 Host Command Interface Busy Status (Read Only)
This bit indicates whether the Host Command interface is busy.
When this bit = 0b, the Host Command interface is idle (not busy).
When this bit = 1b, the Host Command interface is busy.

bit 4 SDRAM Controller Busy Status (Read Only)
This bit indicates whether the SDRAM controller is busy.
When this bit = 0b, the SDRAM controller is idle (not busy).
When this bit = 1b, the SDRAM controller is busy.

bit 3 Host Memory Access Busy Status (Read Only)
This bit indicates the status of the current Host Memory Access. For write accesses, this bit remains at 1b until the memory operation is complete. For read accesses, this bit remains at 1b until the read data has been transferred into the FIFO.
When this bit = 0b, a Host Memory Access is not taking place (not busy).
When this bit = 1b, a Host Memory Access is taking place (busy).

bit 2 Display Engine Busy Status (Read Only)
This bit indicates whether the Display Engine is busy.
When this bit = 0b, the Display Engine is idle (not busy).
When this bit = 1b, the Display Engine is busy.

bit 1 SDRAM Initialized (Read Only)
This bit indicates whether the SDRAM has been initialized. The SDRAM initialization sequence is triggered by the SDRAM Initialization Trigger bit, REG[0102h] bit 0.
When this bit = 0b, the SDRAM has not been initialized.
When this bit = 1b, the SDRAM has been initialized.

bit 0 PLL Lock (Read Only)
This bit indicates whether the PLL output is stable (locked). The S1D13521 synchronous registers (see Table 21-3: “Register Mapping,” on page 159) and the external SDRAM must not be accessed before the PLL output is stable.
When this bit = 0b, the PLL output is not stable.
When this bit = 1b, the PLL output is stable.

Note
SLP mode should always be entered using the SLP command.

A.3.2 Clock Configuration Registers

REG[0010h] PLL Configuration Register 0
Default = 0000h Read/Write

15	14	13	12	11	10	9	8
Reserved							
7	6	5	4	3	2	1	0
n/a		M Divider bits 5-0					

Note
The value of this register should not be changed while the PLL is active, REG[0016h] bit 1 = 0b.

bits 15-8 Reserved
These bits must be set to 00h.

bits 5-0 M Divider bits [5:0]
These bits determine the PLL Lock time (see REG[000Ah] bit 0) when PLL Power Down is disabled, REG[0016h] bit 1 = 0b. The S1D13521 PLL requires a Maximum Lock time of 200us. These bits must be set based on the period of the input clock from the external CLKI or OSC according to the following formula.

$$\mathrm{MDividerBits} = \mathrm{roundup}\left(\frac{200\mathrm{us}}{2048 \times \mathrm{ExternalCLKPeriodInMicroSeconds}}\right)$$

REG[0012h] PLL Configuration Register 1
Default = 0000h Read/Write

15	14	13	12	11	10	9	8
VCO Kv Setting bits 3-0				Reserved			
7	6	5	4	3	2	1	0
Reserved					n/a	Reserved	

Note
The value of this register should not be changed while the PLL is active, REG[0016h] bit 1 = 0b.

bits 15-12 VCO Kv Setting bits [3:0]
These bits must be set according to the frequency of the PLL Output (POUT), in MHz.
When 100MHz ≤ POUT < 120MHz, set these bits to 0100b.
When 120MHz ≤ POUT ≤ 133MHz, set these bits to 0101b.
All other values are Reserved.

bits 11-8 Reserved
These bits must be set to 1001b (9h).

bits 7-3 Reserved
These bits must be set to 0_1001b (09h).

bits 1-0 Reserved
These bits must be set to 01b.

REG[0014h] PLL Configuration Register 2							
Default = 0040h							Read/Write
n/a	Reserved						
15	14	13	12	11	10	9	8
NN Setting bits 3-0				Reserved		Reserved	
7	6	5	4	3	2	1	0

Note
The value of this register should not be changed while the PLL is active, REG[0016h] bit 1 = 0b.

bits 14-8 Reserved
These bits must be set to 000_0000b.

bits 7-4 NN Setting bits [3:0]
These bits are the frequency multiplier used to determine the PLL Output frequency. The PLL output frequency is calculated using the following formula.

fPOUT = (REG[0014h] bits 7-4 + 1) x Input Clock Frequency

The following table provides some example PLL configurations.

Table 21-7 PLL Setting Examples

Input Clock (MHz)	M-Divider (REG[10h] bits 5-0)	NN Setting (REG[14h] bits 7-4)	VCO Kv Setting (REG[12h] bits 15-12)	fVCO (MHz)	fPOUT (MHz)
20	3	5	5	240	120
21	3	5	5	252	126
22	3	5	5	264	132
24	3	4	5	240	120
25	3	4	5	250	125
26.6	3	4	5	266	133
28	3	3	4	224	112
29	3	3	4	232	116

bits 3-2 Reserved
These bits must be set to 00b.

bits 1-0 Reserved
These bits must be set to 00b.

REG[0016h] Clock Configuration Register
Default = 0003h — Read/Write

15	14	13	12	11	10	9	8
n/a							System Clock Divide Select
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
n/a						PLL Power Down Enable	PLL Bypass Mode Enable

bit 8 System Clock Divide Select

This bit selects the divide ratio used to generate the system clock which is derived from either the PLL output or the CLKI input depending on the PLL Bypass Select bit, REG[0016h] bit 0. The maximum frequency for the system clock is 66.5Mhz. For further details on the clock structure, see Chapter 7, “Clocks” on page 50.

When this bit = 0b, the divide ratio is 2:1.

When this bit = 1b, the divide ratio is 3:1.

Note

The value of this bit should not be changed while the PLL is active, REG[0016h] bit 1 = 0b.

bit 1 PLL Power Down Enable

This bit controls the PLL. Once the PLL is placed in a powered down state, enabling it will require a minimum of 1 ms before the PLL output is stable. The status of the PLL can be checked using the PLL Lock bit, REG[000Ah] bit 0. For further details on the clock structure, see Chapter 7, “Clocks” on page 50.

When this bit = 0b, the PLL is in active mode and PLL output is stable once REG[000Ah] bit 0 = 1b.

When this bit = 1b, the PLL is in power down mode. (default)

bit 0 PLL Bypass Mode Enable

This bit controls PLL Bypass Mode which determines whether the PLL output or the CLKI input is used as the internal clock. For further details on the clock structure, see Chapter 7, “Clocks” on page 50.

When this bit = 0b, PLL Bypass Mode is disabled (PLL output is used).

When this bit = 1b, PLL Bypass Mode is enabled (CLKI is used).

REG[0018h] Pixel Clock Configuration Register
Default = 0000h — Read/Write

15	14	13	12	11	10	9	8
n/a							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
n/a			Pixel Clock Divide Disable	Pixel Clock Divide Select bits 3-0			

bit 4 Pixel Clock Divide Disable

This bit controls whether the pixel clock source is divided or not.

When this bit = 0b, the Pixel Clock Divide Select bits (REG[0018h] bits 3-0) are used to determine the pixel clock.

When this bit = 1b, the pixel clock source is not divided (1:1). Note that this setting is not recommended for normal operations.

bits 3-0 Pixel Clock Divide Select bits [3:0]

These bits select the divide ratio for the Pixel Clock which is derived from either the PLL output or CLKI depending on the PLL Bypass Mode Enable bit, REG[0016h] bit 0. For further details on the clock structure, see Chapter 7, “Clocks” on page 50.

Table 21-8: Pixel Clock Divide Ratio Selection

REG[0018h] bits 3-0	Pixel Clock Divide Ratio
0000b	1.5:1
0001b	2:1
0010b	3:1
0011b	4:1
0100b	5:1
0101b	6:1
0110b	7:1
0111b	8:1

REG[0018h] bits 3-0	Pixel Clock Divide Ratio
1000b	9:1
1001b	10:1
1010b	11:1
1011b	12:1
1100b	13:1
1101b	14:1
1110b	16:1
1111b	64:1

REG[001Ah] I2C Thermal Sensor Clock Configuration Register

Default = 0000h Read/Write

15	14	13	12	11	10	9	8
n/a							

7	6	5	4	3	2	1	0
n/a				I2C Thermal Sensor Clock Divide Select bits 3-0			

bits 3-0 I2C Thermal Sensor Clock Divide Select bits [3:0]

These bits select the divide ratio for the I2C Thermal Sensor Clock which is derived from either the PLL output or CLKI depending on the PLL Bypass Mode Enable bit, REG[0016h] bit 0. For further details on the clock structure, see Chapter 7, “Clocks” on page 50.

The divide ratio is calculated using the following formula.

I2C Thermal Sensor Clock Divide Ratio = ((REG[001Ah] bits 3-0 + 1) x 32) : 1

Note

The I2C clock divide ratio must be set such that the output timing meets the requirements of the thermal sensor used.

A.3.3 Component Configuration

REG[0020h] Peripheral Device Configuration Register
Default = 0000h Read/Write

n/a							
15	14	13	12	11	10	9	8
n/a						Big Endian Memory Load Enable	Power Line Management Select
7	6	5	4	3	2	1	0

bit 1 Big Endian Memory Load Enable
This bit selects the load format for read/write accesses to memory. For pixel mapping information, see 11.2, “Host Interface Packed Pixel Data Transfer Format Endian Formatting” on page 97.
When this bit = 0b, Little Endian memory load format is selected.
When this bit = 1b, Big Endian memory load format is selected.

bit 0 Power Line Management Select
This bit selects whether internally generated timing is used for power pin management or whether a 3-wire Active Matrix Power Management IC is used power management. This bit must be set to 0b when a 3-wire Active Matrix Power Management IC is not present.
When this bit = 0b, internal timing is used for power pin management.
When this bit = 1b, a 3-wire Active Matrix Power Management IC is used for power management.

A.3.4 Memory Controller Configuration

REG[0100h] SDRAM Configuration Register
Default = 5070h — Read/Write

SDRAM Power Down Disable	SDRAM Refresh Cycle Time bits 2-0			SDRAM Refresh Rate bits 1-0		SDRAM Row Active Time bits 1-0	
15	14	13	12	11	10	9	8
16-bit SDRAM Enable	SDRAM tRP Latency Select	SDRAM tRCD Latency Select	SDRAM tCL Latency Select	n/a	SDRAM Column Address Count bits 1-0		SDRAM Burst Type Select
7	6	5	4	3	2	1	0

bit 15 SDRAM Power Down Disable
This bit controls the SDRAM power down function which dynamically disables the SDRAM clock when the SDRAM is idle.
When this bit = 0b, the SDRAM power down function is enabled.
When this bit = 1b, the SDRAM power down function is disabled.

bits 14-12 SDRAM Refresh Cycle Time bits [2:0]
These bits specify the guaranteed SDRAM Refresh Cycle Time (tRFC) using the following formula.

Refresh cycle time = REG[0100h] bits 14-12 + 4

bits 11-10 SDRAM Refresh Rate bits [1:0]
These bits specify the SDRAM refresh rate for 8192 rows.

Table 21-9 : SDRAM Refresh Rate Selection

REG[0100h] bits 11-10	Refresh Rate
00b	64 ms
01b	128 ms
10b	256 ms
11b	512 ms

bits 9-8 SDRAM Row Active Time bits [1:0]
These bits specify the Row Active Time (tRAS) which defines the minimum time for an opened row to be issued a precharge.

Table 21-10 : SDRAM Row Active Time (tRAS) Selection

REG[0100h] bits 9-8	Row Active Time
00b	5 clocks
01b	Reserved
10b	6 clocks
11b	7 clocks

bit 7 16-bit SDRAM Enable

This bit specifies whether 16 or 32-bit SDRAM is selected. For a summary of the possible SDRAM sizes, see Table 21-13 “SDRAM Size Selection,” on page 176.

When this bit = 0b, 32-bit SDRAM mode is selected.

When this bit = 1b, 16-bit SDRAM mode is selected.

Note

This bit should not be changed after the SDRAM has been initialized.

bit 6 SDRAM tRP Latency Select

This bit selects the Row Precharge Time which is the precharge time required before a row can be activated again.

When this bit = 0b, the row precharge time is 2 clocks.

When this bit = 1b, the row precharge time is 3 clocks.

bit 5 SDRAM tRCD Latency Select

This bit selects the Row to Column Latency.

When this bit = 0b, the row to column latency is 2 clocks.

When this bit = 1b, the row to column latency is 3 clocks.

bit 4 SDRAM tCL Latency Select

This bit selects the Column Read to Data Available Latency.

When this bit = 0b, the column read to data available latency is 2 clocks.

When this bit = 1b, the column read to data available latency is 3 clocks.

bits 2-1 SDRAM Column Address Count bits [1:0]

This bit specifies the number of column addresses used for the SDRAM.

Table 21-11 : SDRAM Column Address Count Selection

REG[0100h] bits 2-1	Column Address Count
00b	256
01b	512
10b	1024
11b	2048

bit 0 SDRAM Burst Type Select

This bit selects the type of burst used for SDRAM accesses.

When this bit = 0b, full page burst is selected. This setting is used for standard SDRAM.

When this bit = 1b, fixed 8-burst is selected. This setting is used for mobile SDRAM.

REG[0102h] SDRAM Init Register
Default = 0000h — Read/Write

15	14	13	12	11	10	9	8
n/a							SDRAM Initialization Complete (RO)
7	6	5	4	3	2	1	0
n/a						Reserved	SDRAM Initialization Trigger (WO)

bit 8 SDRAM Initialization Complete (Read Only)
This bit indicates the initialization status of the SDRAM. Once SDRAM has been initialized, this bit will remain high until the S1D13521 is reset.
When this bit = 0b, the SDRAM has not been initialized.
When this bit = 1b, the SDRAM has been initialized.

bit 1 Reserved
This bit must be set to 1b.

bit 0 SDRAM Initialization Trigger (Write Only)
This bit triggers the SDRAM initialization sequence and should only be used after a reset. The initialization status of the SDRAM is indicated by the SDRAM Initialization Complete bit, REG[0102h] bit 8.
Writing a 0b to this bit has no effect.
Writing a 1b to this bit initiates the SDRAM initialization sequence.

REG[0104h] SDRAM State Trigger Register
Default = 0000h — Read/Write

15	14	13	12	11	10	9	8
n/a							SDRAM Self Refresh Mode State (RO)
7	6	5	4	3	2	1	0
n/a						SDRAM Exit Self Refresh Trigger (WO)	SDRAM Enter Self Refresh Trigger (WO)

bit 8 SDRAM Self Refresh Mode State (Read Only)
This bit indicates whether the SDRAM is in Self Refresh mode or not.
When this bit = 0b, the SDRAM is not in self refresh mode (normal operating mode).
When this bit = 1b, the SDRAM is in self refresh mode.

Note
The memory must not be accessed while the SDRAM is in self refresh mode. To read or write memory, self refresh mode must be exited, REG[0104h] bit 1 = 1b.

bit 1 SDRAM Exit Self Refresh Trigger (Write Only)
This bit triggers the sequence that removes (exits) the SDRAM from Self Refresh mode.
Writing a 0b to this bit has no effect.
Writing a 1b to this bit triggers the exit self refresh sequence.

Note
The memory must not be accessed while the SDRAM is in self refresh mode. To read or write to memory, self refresh mode must be exited, REG[0104h] bit 1 = 1b.

bit 0 SDRAM Enter Self Refresh Trigger (Write Only)
This bit triggers the sequence to places (enters) the SDRAM to Self Refresh mode.
Writing a 0b to this bit has no effect.
Writing a 1b to this bit triggers the enter self refresh sequence.

REG[0106h] SDRAM Refresh Clock Configuration Register
Default = 0177h Read/Write

SDRAM Refresh Clock Divide Select bits 15-8							
15	14	13	12	11	10	9	8
SDRAM Refresh Clock Divide Select bits 7-0							
7	6	5	4	3	2	1	0

bits 15-0 SDRAM Refresh Clock Divide Select bits [15:0]
These bits select the divide used to determine the SDRAM Refresh Clock frequency. These bits should be set such that the resulting refresh clock is approximately 64KHz. For further information on the clock structure, see Chapter 7, “Clocks” on page 50.

Refresh Clock Divide = REG[0106h] bits 15-0 + 1

The refresh clock is calculated using the following formula.

Refresh clock frequency = CLKI frequency ÷ Refresh Clock Divide

For example, the default register value of 0177h results in the following refresh frequency when CLKI is 24MHz.

Refresh clock frequency = 24MHz ÷ 375
= 64KHz

REG[0108h] SDRAM Read Data Tap Delay Select Register
Default = 0088h Read/Write

n/a							
15	14	13	12	11	10	9	8
Reserved	n/a	SDRAM Read Data Sampling Select	SDRAM Read Data Sampling Clock Invert Enable	Reserved	Reserved		
7	6	5	4	3	2	1	0

bit 7 Reserved
This bit must be set to 1b.

bit 5 SDRAM Read Data Sampling Select
This bit selects when SDRAM read data is sampled.
When this bit = 0b, SDRAM read data is sampled on the positive edge.
When this bit = 1b, SDRAM read data is sampled on the negative edge.

bit 4 SDRAM Read Data Sampling Clock Invert Enable
This bit controls whether the sampling clock used for SDRAM data reads is inverted.
When this bit = 0b, the sampling clock is not inverted.
When this bit = 1b, the sampling clock is inverted.

bit 3 Reserved
This bit must be set to 0b.

bits 2-0 Reserved
These bits must be set to 000b.

REG[010Ah] SDRAM Extended Mode Configuration Register
Default = 0000h Read/Write

n/a	SDRAM Driver Strength bits 1-0		Temperature Compensated Self Refresh bits 1-0		Partial Array Self Refresh bits 2-0		
15	14	13	12	11	10	9	8
n/a					SDRAM Size bits 1-0		Extended Mode Register Program on Initialization Enable
7	6	5	4	3	2	1	0

bits 14-13 SDRAM Driver Strength bits [1:0]
These bits only have an effect when the Extended Mode Register Program On Initialization Enable bit is set to 1b, REG[010Ah] bit 0 = 1b. These bits set the value for Driver Strength (DS) that is programmed into the extended mode register of the mobile SDRAM.

Table 21-12 : SDRAM Driver Strength Selection

REG[010Ah] bits 14-13	Driver Strength
00b	Full Strength
01b	Half Strength
10b	Quarter Strength
11b	Eighth Strength

bits 12-11 Temperature Compensated Self Refresh bits [1:0]
These bits only have an effect when the Extended Mode Register Program On Initialization Enable bit is set to 1b, REG[010Ah] bit 0 = 1b. Mobile SDRAM allows the self refresh rate to be varied based on the temperature of the SDRAM. These bits set the value for Temperature Compensated Self Refresh (TCSR) that is programmed into the extended mode register of the mobile SDRAM.

bits 10-8 Partial Array Self Refresh bits [2:0]
These bits only have an effect when the Extended Mode Register Program On Initialization Enable bit is set to 1b, REG[010Ah] bit 0 = 1b. These bits set the value for Partial Array Self Refresh (PASR) that is programmed into the extended mode register of the mobile SDRAM.

bits 2-1 SDRAM Size bits [1:0]

These bits specify the SDRAM size, in M bytes. The SDRAM size differs based on the setting of the 16-bit SDRAM Enable bit, REG[0100h] bit 7. This setting is used for bank address placement.

Table 21-13 : SDRAM Size Selection

REG[010Ah] bits 2-1	SDRAM Size for 32-bit SDRAM (REG[0100h] bit 7 = 0b)	SDRAM Size for 16-bit SDRAM (REG[0100h] bit 7 = 1b)
00b	8M bytes	4M bytes
01b	16M bytes	8M bytes
10b	32M bytes	16M bytes
11b	64M bytes	32M bytes

bit 0 Extended Mode Register Program On Initialization Enable

When mobile SDRAM is used, this bit controls whether the extended mode register is programmed when the SDRAM is initialized, REG[0102h] bit 0 = 1b.

When this bit = 0b, the extended mode register is not programmed when the SDRAM is initialized.

When this bit = 1b, the extended mode register is programmed when the SDRAM is initialized.

REG[010Ch] SDRAM Controller Software Reset Register

Default = not applicable Write Only

15	14	13	12	11	10	9	8
n/a							

7	6	5	4	3	2	1	0
n/a							SDRAM Controller Software Reset

bit 0 SDRAM Controller Software Reset (Write Only)

This bit performs a software reset of the SDRAM controller.

Writing a 0b to this bit has no effect.

Writing a 1b to this bit performs a software reset of the SDRAM controller.

A.3.5 Host Interface Memory Access Configuration

REG[0140h] Host Memory Access Configuration and Status Register
Default = 0000h — Read/Write

15	14	13	12	11	10	9	8
Host Memory Interface Reset (WO)	n/a	Host Memory Interface Ready Status (RO)	Host Memory Interface Busy Status (RO)	n/a		Write Rotation Select bits 1-0	
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Packed Pixel Destination Start Address Select	n/a	Host Packed Pixel Select bits 1-0		Host Rotate 0 and 180 Line Buffer Bypass Enable	Memory Read/Write Select	Memory Access Type Select bits 1-0	

bit 15 Host Memory Interface Reset (Write Only)
This bit performs a software reset of the host memory interface.
Writing a 0b to this bit has no effect.
Writing a 1b to this bit initiates a software reset of the host memory interface.

bit 13 Host Memory Interface Ready Status (Read Only)
This bit indicates the ready status of the host memory interface once a data transfer has been triggered (see REG[0142h] bit 0).
When this bit = 0b, the host memory interface is not ready (busy filling or clearing the buffer).
When this bit = 1b, the host memory interface is ready for a data transfer.

Note
For read operations, the Host should read from REG[0154h] one more time after this bit goes to 0b.

bit 12 Host Memory Interface Busy Status (Read Only)
This bit indicates the busy status of the host memory interface.
When this bit = 0b, the host memory interface is idle.
When this bit = 1b, the host memory interface is busy.

bits 9-8 Write Rotation Select bits [1:0]
These bits only have an effect when Packed Pixel Access is selected, REG[0140h] bits 1-0 = 00b. These bits select the counter-clockwise rotation applied to host memory interface writes.

Table 21-14 : Write Rotation Selection

REG[0140h] bits 9-8	Write Rotation
00b	0°
01b	90°
10b	180°
11b	270°

bit 7

Packed Pixel Destination Start Address Select
When packed pixel mode is selected (REG[0140h] bits 1-0 = 00b), this bit determines the destination start address for the memory write.
When this bit = 0b, the destination start address is defined by the Display Engine image buffer start address, REG[0310h] ~ REG[0312h].
When this bit = 1b, the destination start address is defined by the Host raw memory access address, REG[0144h] ~ REG[0146h].

bits 5-4

Host Packed Pixel Select bits [1:0]
These bits only have an effect when Packed Pixel Access is selected, REG[0140h] bits 1-0 = 00b. These bits select the packed pixel mode used for host memory interface accesses.

Table 21-15 : Packed Pixel Mode Selection

REG[0140h] bits 5-4	Packed Pixel Mode
00b	2 bpp
01b	3 bpp
10b	4 bpp
11b	1 Byte-per-pixel

Note
These bits must be set to 1 Byte-per-pixel (11b) when a Big Endian raw memory write is performed (REG[0020h] bit 1 = 1b and REG[0140h] bits 1-0 = 01b).

bit 3

Host Rotate 0 and 180 Line Buffer Bypass Enable
When the Write Rotation Select bits are set for 0° or 180° (REG[0140h] bits 9-8 = 00b or 10b), this bit determines whether the line buffer is used or bypassed. When write rotation is set for 90° or 270°, the line buffer is always used.
When this bit = 0b, the line buffer is used.
When this bit = 1b, the line buffer is bypassed (not used).

bit 2

Memory Read/Write Select
This bit selects the memory read/write direction.
When this bit = 0b, the host memory interface is configured to write to memory.
When this bit = 1b, the host memory interface is configured to read from memory.

bits 1-0

Memory Access Type Select bits [1:0]
These bits select the type of memory access performed through the host memory interface.

Table 21-16 : Memory Access Type Selection

REG[0140h] bits 1-0	Memory Access Type
00b	Packed Pixel Access (Write Only)
01b	Raw Memory Access (Read/Write)
10b ~ 11b	Reserved

Note
For a line data length (horizontal display size, see REG[0306h]) greater than 2048, only raw memory writes are supported.

REG[0142h] Host Memory Access Triggers Register
Default = not applicable — Write Only

15	14	13	12	11	10	9	8
n/a							
7	6	5	4	3	2	1	0
n/a						Host Transfer Stop Trigger	Host Transfer Start Trigger

bit 1 Host Transfer Stop Trigger (Write Only)
This bit stops the data transfer taking place on the host memory interface.
Writing a 0b to this bit has no effect.
Writing a 1b to this bit triggers the current host memory interface transfer to stop.

Note
Any memory operation in progress should be terminated with this bit before a new memory operation is initiated.

bit 0 Host Transfer Start Trigger (Write Only)
This bit starts a new data transfer on the host memory interface.
Writing a 0b to this bit has no effect.
Writing a 1b to this bit triggers a new data transfer to start on the host memory interface.

REG[0144h] Host Raw Memory Access Address Register 0
Default = 0000h — Read/Write

15	14	13	12	11	10	9	8
Host Raw Memory Access Address bits 15-8							
7	6	5	4	3	2	1	0
Host Raw Memory Access Address bits 7-0 (bit 0 is always 0b)							

REG[0146h] Host Raw Memory Access Address Register 1
Default = 0000h — Read/Write

15	14	13	12	11	10	9	8
Reserved						Host Raw Memory Access Address bits 25-24	
7	6	5	4	3	2	1	0
Host Raw Memory Access Address bits 23-16							

REG[0146h] bits 15-10 Reserved
The default value for these bits is 00_0000b.

REG[0146h] bits 9-0
REG[0144h] bits 15-0 Host Raw Memory Access Address bits [25:0]
These bits are only used for raw memory accesses (REG[0140h] bits 1-0 = 01b). These bits specify the 26-bit memory address used for raw memory accesses by the host memory interface. For raw memory reads/writes, the starting address must be on a 16-bit boundary.

Note
1. The Host Raw Memory Access Address must be set within the available memory range.
2. If the Host Raw Memory Access Address is used for a packed pixel write operation (REG[0140h] bit 7 = 0b and bits 1-0 = 00b), the address specified in these bits must be 64-bit aligned.

REG[0148h] Host Raw Memory Access Count Register 0
Default = 0000h Read/Write

Host Raw Memory Access Count bits 15-8							
15	14	13	12	11	10	9	8
Host Raw Memory Access Count bits 7-0							
7	6	5	4	3	2	1	0

REG[014Ah] Host Raw Memory Access Count Register 1
Default = 0000h Read/Write

Reserved						Host Raw Memory Access Count bits 25-24	
15	14	13	12	11	10	9	8
Host Raw Memory Access Count bits 23-16							
7	6	5	4	3	2	1	0

REG[014Ah] bits 15-10 Reserved

The default value for these bits is 00_0000b.

REG[014Ah] bits 9-0
REG[0148h] bits 15-0 Host Raw Memory Access Count bits [25:0]

These bits are only used for raw memory accesses (REG[0140h] bits 1-0 = 01b). These bits are programmed before the start of a host memory operation to specify the number of 16-bit accesses that will be performed for raw memory accesses by the host memory interface during burst operations. The minimum number of raw memory accesses that can be performed is 1.

During a host memory access, these bits can be used with the following formulas to determine the number of 16-bit accesses remaining for the current memory access.
For write access, REG[0148h] ~ REG[014Ah] = number of words left to be written.
For read access, REG[0148h] ~ REG[014Ah] = number of words left to be read -1.

For raw memory access reads, the access count must be set to the required number of reads + 1. Once the read operation is complete, the host memory interface should be reset (REG[0140h] bit 15 = 1b).

Note

1. These bits must be set such that the Host Memory Access operation is within the configured memory range.
2. These bits must not be set to 0000_0000h for a Host memory access.

REG[014Ch] Packed Pixel Rectangular X-Start Register
Default = 0000h Read/Write

n/a			Reserved	Packed Pixel Rectangular X-Start Position bits 11-8			
15	14	13	12	11	10	9	8
Packed Pixel Rectangular X-Start Position bits 7-0							
7	6	5	4	3	2	1	0

bit 12 Reserved
The default value for this bit is 0b.

bits 11-0 Packed Pixel Rectangular X-Start Position bits [11:0]
These bits are only used for packed pixel accesses (REG[0140h] bits 1-0 = 00b). These bits specify the X-Start position of the image write, in pixels, relative to the top left corner of the display area. For further information, see 10.1, “Introduction” on page 79.

Note
For 0° and 180° rotation (REG[0140h] bits 9-8 = 00b or 10b), the X-Start position must be set smaller than the line data length, REG[0306h] bits 12-0.
For 90° and 270° rotation (REG[0140h] bits 9-8 = 01b or 11b), the X-Start position must be set smaller than the frame data length, REG[0300h] bits 12-0.

Note
When 0° or 180° write rotation is selected (REG[0140h] bits 9-8 = 00b or 10b), the following X-Start position limitations must be observed.

Table 21-17 : X-Start Position Limitations for 0° or 180° Write Rotation

REG[0140h] bits 9-8	Packed Pixel Mode	X-Start Position Limitation
00b	2 bpp	Must be divisible by 8 pixels
01b	3 bpp	Must be divisible by 4 pixels
10b	4 bpp	Must be divisible by 4 pixels
11b	1 Byte-per-pixel	Must be divisible by 2 pixels

REG[014Eh] Packed Pixel Rectangular Y-Start Register
Default = 0000h Read/Write

n/a			Reserved	Packed Pixel Rectangular Y-Start Position bits 11-8			
15	14	13	12	11	10	9	8
Packed Pixel Rectangular Y-Start Position bits 7-0							
7	6	5	4	3	2	1	0

bit 12 Reserved
The default value for this bit is 0b.

bits 11-0 Packed Pixel Rectangular Y-Start Position bits [11:0]
These bits are only used for packed pixel accesses (REG[0140h] bits 1-0 = 00b). These bits specify the Y-Start position of the image write, in pixels, relative to the top left corner of the display area. For further information, see 10.1, “Introduction” on page 79.

Note
For 0° and 180° rotation (REG[0140h] bits 9-8 = 00b or 10b), the Y-Start position must be set smaller than the frame data length, REG[0300h] bits 12-0.
For 90° and 270° rotation (REG[0140h] bits 9-8 = 01b or 11b), the Y-Start position must be set smaller than the line data length, REG[0306h] bits 12-0.

REG[0150h] Packed Pixel Rectangular Width Register
Default = 0000h Read/Write

n/a			Packed Pixel Rectangular Width bits 12-8				
15	14	13	12	11	10	9	8
Packed Pixel Rectangular Width bits 7-0							
7	6	5	4	3	2	1	0

bits 12-0 Packed Pixel Rectangular Width bits [12:0]
These bits are only used for packed pixel accesses (REG[0140h] bits 1-0 = 00b). These bits specify the width of the image write, in pixels. For further information, see 10.1, “Introduction” on page 79.

REG[0152h] Packed Pixel Rectangular Height Register
Default = 0000h Read/Write

n/a			Packed Pixel Rectangular Height bits 12-8				
15	14	13	12	11	10	9	8
Packed Pixel Rectangular Height bits 7-0							
7	6	5	4	3	2	1	0

bits 12-0 Packed Pixel Rectangular Height bits [12:0]
These bits are only used for packed pixel accesses (REG[0140h] bits 1-0 = 00b). These bits specify the height of the image write, in pixels. For further information, see 10.1, “Introduction” on page 79.

REG[0154h] Host Memory Access Port Register
Default = 0000h — Read/Write

15	14	13	12	11	10	9	8
Host Memory Access Port bits 15-8							
7	6	5	4	3	2	1	0
Host Memory Access Port bits 7-0							

bits 15-0 Host Memory Access Port bits [15:0]
These bits are the data port for host memory interface accesses.

REG[0156h] Host Memory Checksum Register
Default = 0000h — Read/Write

15	14	13	12	11	10	9	8
Host Memory Checksum bits 15-8							
7	6	5	4	3	2	1	0
Host Memory Checksum bits 7-0							

bits 15-0 Host Memory Checksum bits [15:0]
These bits are only used for host memory writes.
These bits contain a checksum value of all 16-bit memory accesses. After each 16-bit memory access, the data value is added to the value in this register. The checksum value is reset to 0000h when a host transfer start is triggered, REG[0142h] bits 0 = 1b.

To manually reset the checksum calculation, the Host must write 0000h to these bits.

REG[0158h] Host Raw Memory FIFO Level Register
Default = 0000h — Read Only

15	14	13	12	11	10	9	8
n/a							Reserved
7	6	5	4	3	2	1	0
Reserved			Host Raw Memory FIFO Level bits 4-0				

bits 8-5 Reserved
The default value for these bits is 0000b.

bits 4-0 Host Raw Memory FIFO Level bits [4:0] (Read Only)
These bits indicate the FIFO Level in 16-bit word spaces. For write mode, these bits indicate the number of spaces available for write data. For read mode, these bits indicate the number of words that are available to be read - 1. The maximum number of FIFO spaces is 16.

A.3.6 SPI Flash Memory Interface

REG[0200h] SPI Flash Read Data Register
Default = 0000h — Read Only

15	14	13	12	11	10	9	8
n/a							
7	6	5	4	3	2	1	0
SPI Flash Read Data bits 7-0							

bits 7-0 SPI Flash Read Data bits [7:0] (Read Only)
These bits contain the 8-bit data value received from the SPI Flash Memory. A read data transfer is triggered by a “dummy” write to REG[0202h] where bit 8 = 0b.

Note
If a Fast Read command is used for the SPI Flash, a dummy read from this register must be performed for the dummy read cycle required by the SPI Flash.

REG[0202h] SPI Flash Write Data Register
Default = not applicable — Write Only

15	14	13	12	11	10	9	8
n/a							SPI Flash Data Output Enable
7	6	5	4	3	2	1	0
SPI Flash Write Data bits 7-0							

Note
This register should only be accessed when the SPI Flash Access Mode is set for Host Register access mode, REG[0204h] bit 7 = 0b.

Note
This register should not be written to when the SPI Flash Chip Select is disabled, REG[0208h] bit 0 = 0b.

bit 8 SPI Flash Data Output Enable (Write Only)
This bit determines whether a read or write data transfer takes place on the SPI Flash Memory interface.
When this bit = 0b, a read data transfer from the SPI Flash Memory takes place. The read data transfer is triggered by a “dummy” write to REG[0202h].
When this bit = 1b, a write data transfer to the SPI Flash Memory takes place.

bits 7-0 SPI Flash Write Data bits [7:0] (Write Only)
These bits are the write data register for the SPI Flash Memory. A write data transfer is triggered by a write to REG[0202h] where bit 8 = 1b. When the status flag for this register shows empty, the CPU is permitted to write data into this register.

REG[0204h] SPI Flash Control Register Default = 0099h							Read/Write
n/a							
15	14	13	12	11	10	9	8
SPI Flash Access Mode Select	SPI Flash Read Command Select	SPI Flash Clock Divide Select bits 2-0			SPI Flash Clock Phase Select	SPI Flash Clock Polarity Select	SPI Flash Enable
7	6	5	4	3	2	1	0

bit 7 SPI Flash Access Mode Select

This bit selects between Display Engine access mode and Host Register access mode. This bit must be set to 1b before performing a Display Engine operation to allow the Display Engine to communicate with SPI Flash Memory.

When this bit = 0b, Host Register access mode is selected.

When this bit = 1b, Display Engine access mode is selected.

bit 6 SPI Flash Read Command Select

This bit selects which serial flash command is used for reading data and depends on the SPI Flash Memory device. Please refer to the device data sheet to determine which setting is appropriate.

When this bit = 0b, the serial flash read speed is Low.

When this bit = 1b, the serial flash read speed is High.

Note

1. This bit is only used for Display Engine access mode, REG[0204h] bit 7 = 1b.
2. The Flash Memory must support the Fast Read command. For detailed Flash Memory requirements, see 17.3, “Serial Flash Memory” on page 136.

bits 5-3 SPI Flash Clock Divide Select bits [2:0]

These bits select the divide ratio for the SPI Flash Clock which is derived from either the PLL output or CLKI depending on the setting of the PLL Bypass Mode Enable bit, REG[0016h] bit 0. For further details on the clock structure, see Chapter 7, “Clocks” on page 50.

Table 21-18: SPI Flash Clock Divide Ratio Selection

REG[0204h] bits 5-3	SPI Flash Clock Divide Ratio	REG[0204h] bits 5-3	SPI Flash Clock Divide Ratio
000b	2:1	100b	6:1
001b	3:1	101b	7:1
010b	4:1	110b	8:1
011b	5:1	111b	9:1

Note

For odd SPI Flash Clock divide ratio settings, SPICLK will not have a 50% duty cycle.

bit 2 SPI Flash Clock Phase Select

This bit selects the SPI Flash clock phase. For a summary of the SPI Flash Memory clock phase and polarity settings, see Table 21-19 “SPI Flash Clock Phase and Polarity,” on page 186.

bit 1 SPI Flash Clock Polarity Select (CPOL)

This bit selects the SPI Flash clock polarity. The following table summarizes the SPI Flash clock polarity and phase settings.

Table 21-19 : SPI Flash Clock Phase and Polarity

REG[0204h] bit 2	REG[0204h] bit 1	Valid Data	Clock Idling Status
0b	0b	Rising edge of SPI Flash Clock	Low
	1b	Falling edge of SPI Flash Clock	High
1b	0b	Falling edge of SPI Flash Clock	Low
	1b	Rising edge of SPI Flash Clock	High

bit 0 SPI Flash Enable

This bit controls the SPI Flash Memory interface logic.
When this bit = 0b, the SPI Flash Memory interface is disabled.
When this bit = 1b, the SPI Flash Memory interface is enabled.

Note

The SPI Flash Memory interface should be disabled (REG[0204h] bit 0 = 0b) before programming the SPI Flash registers, REG[0200h] ~ REG[0208h].

REG[0206h] SPI Flash Status Register

Default = 0004h Read Only

15	14	13	12	11	10	9	8
n/a							
7	6	5	4	3	2	1	0
n/a				SPI Flash Busy Flag	SPI Flash Write Data Register Empty Flag	SPI Flash Read Data Overrun Flag	SPI Flash Read Data Ready Flag

bit 3 SPI Flash Busy Flag (Read Only)

This bit indicates the status of the SPI Flash Memory interface.
When this bit = 0b, the SPI Flash Memory interface is not busy (idle).
When this bit = 1b, the SPI Flash Memory interface is busy.

bit 2 SPI Flash Write Data Register Empty Flag (Read Only)

This bit indicates when the SPI Flash Write Data register (REG[0202h]) is empty which occurs when data written to the register is latched for serialization/transmission.
When this bit = 0b, the SPI Flash Write Data register is not empty.
When this bit = 1b, the SPI Flash Write Data register is empty. (default)

To clear this flag, write data to the SPI Flash Write Data register, REG[0202h].

bit 1 SPI Flash Read Data Overrun Flag (Read Only)

This bit indicates when new data is loaded into the SPI Flash Read Data register (REG[0200h]) before the existing data has been read (REG[0206h] bit 0 = 1b while the new data is loaded). In this case, the old data is no longer available and must be re-read.
When this bit = 0b, a SPI Flash Read Data overrun has not occurred.
When this bit = 1b, a SPI Flash Read Data overrun has occurred.

To clear this flag, read the SPI Flash Read Data register, REG[0200h].

bit 0 SPI Flash Read Data Ready Flag (Read Only)
This bit indicates when read data from the SPI Flash Memory is available (or ready) in the SPI Flash Read Data register, REG[0200h].
When this bit = 0b, the SPI Flash Memory read data is not ready.
When this bit = 1b, the SPI Flash Memory read data is ready.

To clear this flag, read the SPI Flash Read Data register, REG[0200h].

REG[0208h] SPI Flash Chip Select Control Register
Default = 0000h Read/Write

15	14	13	12	11	10	9	8
n/a							

7	6	5	4	3	2	1	0
n/a							SPI Flash Chip Select Enable

bit 0 SPI Flash Chip Select Enable
This bit controls chip select (SPIDCS_L) for the SPI Flash Memory interface and is used to access the serial EEPROM.
When this bit = 0b, the chip select for the slave device is disabled.
When this bit = 1b, the chip select for the slave device is enabled.

Note

1. The chip select output pin for the Serial Flash Memory interface is active low. Therefore, SPIDCS_L is high when this bit = 0b, and SPIDCS_L is low when this bit = 1b.
2. For Host Register Access Mode (REG[0204h] bit 7 = 0b), this bit is not masked by the SPI Flash Enable bit (REG[0204h] bit 0).

A.3.7 I2C Thermal Sensor Interface Registers

REG[0210h] I2C Thermal Sensor Configuration Register
Default = 0000h — Read/Write

15	14	13	12	11	10	9	8
n/a					I2C Thermal Sensor ID Address bits 2-0		
7	6	5	4	3	2	1	0
n/a							

bits 10-8 I2C Thermal Sensor ID Address bits [2:0]
These bits are the three least significant bits of the I2C thermal sensor ID address, A[2:0]. A[6:3] are fixed to a value of 1001b. The default value for A[2:0] is 000b, resulting in a default ID address of 100_1000b (48h).

REG[0212h] I2C Thermal Sensor Status Register
Default = 0002h — Read Only

15	14	13	12	11	10	9	8
n/a							
n/a		I2C SDA Pin Status	I2C SCL Pin Status	n/a	Reserved	I2C Thermal Sensor ID Status	I2C Thermal Sensor Busy Status
7	6	5	4	3	2	1	0

bit 5 I2C SDA Pin Status (Read Only)
This bit indicates the status of the I2C SDA pin which is used to communicate with the Thermal Sensor.
When this bit = 0b, the I2C SDA pin is low (0).
When this bit = 1b, the I2C SDA pin is high (1).

bit 4 I2C SCL Pin Status (Read Only)
This bit indicates the status of the I2C SCL pin which is used to communicate with the Thermal Sensor.
When this bit = 0b, the I2C SCL pin is low (0).
When this bit = 1b, the I2C SCL pin is high (1).

bit 2 Reserved
The default value for this bit is 0b.

bit 1 I2C Thermal Sensor ID Status (Read Only)
This bit indicates the status of the Thermal Sensor ID transfer.
When this bit = 0b, the thermal sensor ID has been transferred (ACK).
When this bit = 1b, the thermal sensor ID has not been transferred (NACK).

bit 0 I2C Thermal Sensor Busy Status (Read Only)
This bit indicates the status of the I2C Thermal Sensor.
When this bit = 0b, the I2C thermal sensor is idle (not busy).
When this bit = 1b, the I2C thermal sensor is busy.

REG[0214h] I2C Thermal Sensor Read Trigger Register
Default = not applicable — Write Only

15	14	13	12	11	10	9	8
n/a							

7	6	5	4	3	2	1	0
n/a							I2C Thermal Sensor Read Trigger

bit 0 I2C Thermal Sensor Read Trigger (Write Only)
This bit triggers the thermal sensor to read the current temperature which is stored in the I2C Thermal Sensor Temperature Value register, REG[0216h].
Writing a 0b to this bit has no effect.
Writing a 1b to this bit triggers a temperature read from the Thermal Sensor.

REG[0216h] I2C Thermal Sensor Temperature Value Register
Default = 0007h — Read Only

15	14	13	12	11	10	9	8
n/a							

7	6	5	4	3	2	1	0
I2C Thermal Sensor Temperature Value bits 7-0							

bits 7-0 I2C Thermal Sensor Temperature Value bits [7:0] (Read Only)
These bits indicate the temperature value received from the I2C Thermal Sensor after a I2C thermal sensor read has been triggered, REG[0214h] bit 0 = 1b. The temperature value is stored in 2's compliment format.

A.3.8 3-Wire Chip Interface Registers

REG[0220h] 3-Wire Chip Configuration Register
Default = 0000h — Read/Write

15	14	13	12	11	10	9	8
n/a							3-Wire Chip Read/Write Select
7	6	5	4	3	2	1	0
n/a			3-Wire Chip Interface Clock Divide Select bits 4-0				

bit 8 — 3-Wire Chip Read/Write Select
This bit selects whether a read or write operation is performed from/to the 3-Wire chip. A read/write operation is triggered by a write to the 3-Wire Chip Address bits, REG[0224h] bits 7-0.
When this bit = 0b, a write operation is selected (see REG[0224h] bits 15-8).
When this bit = 1b, a read operation is selected (see REG[0226h] bits 7-0).

bits 4-0 — 3-Wire Chip Interface Clock Divide Select bits [4:0]
These bits select the divide ratio used to generate the clock for the 3-Wire Chip interface. The clock is derived from either the PLL output or CLKI depending on the setting of the PLL Bypass Mode Enable bit, REG[0016h] bit 0. For further details on the clock structure, see Chapter 7, “Clocks” on page 50.

Table 21-20: 3-Wire Chip Interface Clock Divide Selection

REG[0200h] bits 4-0	Divide Ratio
0_0000b (00h)	2:1
0_0001b (01h)	4:1
0_0010b ~ 1_1111b (02h ~ 1Fh)	Reserved

REG[0222h] 3-Wire Chip Access Status Register
Default = 0000h — Read Only

15	14	13	12	11	10	9	8
n/a							
7	6	5	4	3	2	1	0
n/a					3-Wire Chip Data Byte Transfer Status	3-Wire Chip Address Byte Send Status	3-Wire Chip Operation Status

bit 2 — 3-Wire Chip Data Byte Transfer Status (Read Only)
This bit indicates the status of the data byte transfer (send/receive) on the 3-Wire Chip interface.
When this bit = 0b, a data byte is not being transferred (not busy).
When this bit = 1b, a data byte is being transferred (busy).

bit 1 — 3-Wire Chip Address Byte Send Status (Read Only)
This bit indicates the status of the address byte transfer (send) on the 3-Wire Chip interface.
When this bit = 0b, an address byte is not being transferred (not busy).
When this bit = 1b, an address byte is being transferred (busy).

bit 0 3-Wire Chip Operation Status (Read Only)
This bit indicates the status of the 3-wire chip interface.
When this bit = 0b, the 3-wire chip interface is idle (not busy).
When this bit = 1b, the 3-wire chip interface is busy.

REG[0224h] 3-Wire Chip Address and Write Data Byte Register
Default = 0000h Read/Write

15	14	13	12	11	10	9	8
3-Wire Chip Write Data bits 7-0							
7	6	5	4	3	2	1	0
3-Wire Chip Address bits 7-0							

bits 15-8 3-Wire Chip Write Data bits [7:0]
These bits specify the data to be written to the 3-Wire Chip during a write operation (REG[0220h] bit 8 = 0b). These bits are not used if a read operation is selected.

bits 7-0 3-Wire Chip Address bits [7:0]
These bits specify the address for the transfer to or from the 3-Wire Chip. A transfer is triggered by a write to these bits.

REG[0226h] 3-Wire Chip Read Data Byte Register
Default = 0000h Read Only

15	14	13	12	11	10	9	8
n/a							
7	6	5	4	3	2	1	0
3-Wire Chip Read Data bits 7-0							

bits 7-0 3-Wire Chip Read Data bits [7:0] (Read Only)
These bits return the data read from the 3-Wire Chip in the previous read operation (REG[0220h] bit 8 = 1b).

A.3.9 Power Pin Control Configuration Registers

Power Pin control uses the PWR[3:0] pins which can be programmed to perform a power-on/off cycle using the Power Pin Timing Delay registers (REG[0234h] ~ REG[0238h]) and the PWRCOM pin which is controlled by the Display Engine. Both PWR[3:0] and PWRCOM can be manually controlled using the bypass option (see REG[0232h]).

REG[0230h] Power Pin Control Register
Default = 0000h — Read/Write

15	14	13	12	11	10	9	8
n/a			PWR3 Pin Status (RO)	PWR2 Pin Status (RO)	PWR1 Pin Status (RO)	PWR0 Pin Status (RO)	PWRCOM Pin Status (RO)
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Power Cycle Busy (RO)	n/a					Power-Off Cycle Trigger (WO)	Power-On Cycle Trigger (WO)

bits 12-9 PWR[3:0] Pin Status (Read Only)
These bits indicates the status of the individual PWR[3:0] pins.
When this bit = 0b, the PWR[3:0] pin is low (0).
When this bit = 1b, the PWR[3:0] pin is high (1).

bit 8 PWRCOM Pin Status (Read Only)
This bit indicates the status of the PWRCOM pin.
When this bit = 0b, the PWRCOM pin is low (0).
When this bit = 1b, the PWRCOM pin is high (1).

bit 7 Power Cycle Busy (Read Only)
This bit indicates whether a power-on/off cycle is currently happening.
When this bit = 0b, a power-on/off cycle is not happening (not busy).
When this bit = 1b, a power-on/off cycle is happening (busy).

bit 1 Power-Off Cycle Trigger (Write Only)
This bit triggers a power-off cycle on the PWR[3:0] pins. Before triggering a power-off cycle, the power pin delay times should be configured using the Power Pin Timing Delay registers, REG[0234h] ~ REG[0238h].
Writing a 0b to this bit has no effect.
Writing a 1b to this bit triggers a a power-off cycle on the PWR[3:0] pins.

bit 0 Power-On Cycle Trigger (Write Only)
This bit triggers a power-on cycle on the PWR[3:0] pins. Before triggering a power-on cycle, the power pin delay times should be configured using the Power Pin Timing Delay registers, REG[0234h] ~ REG[0238h].
Writing a 0b to this bit has no effect.
Writing a 1b to this bit triggers a a power-on cycle on the PWR[3:0] pins.

REG[0232h] Power Pin Configuration Register
Default = 0000h — Read/Write

n/a			PWR3 Pin Bypass Enable	PWR2 Pin Bypass Enable	PWR1 Pin Bypass Enable	PWR0 Pin Bypass Enable	PWRCOM Pin Bypass Enable
15	14	13	12	11	10	9	8
n/a			PWR3 Pin Bypass Value	PWR2 Pin Bypass Value	PWR1 Pin Bypass Value	PWR0 Pin Bypass Value	PWRCOM Pin Bypass Value
7	6	5	4	3	2	1	0

bit 12 PWR3 Pin Bypass Enable
This bit controls PWR3 pin bypass mode which allows the PWR3 pin output value to be set directly. When bypass mode is enabled, the Trigger bits (REG[0230h] bits 1-0) and the Timing Delay bits (REG[0234] ~ REG[0238h]) have no effect.
When this bit = 0b, PWR3 pin bypass mode is disabled.
When this bit = 1b, PWR3 pin bypass mode is enabled and the PWR3 pin output is set to the value specified by the PWR3 Pin Bypass Value, REG[0232h] bit 4.

bit 11 PWR2 Pin Bypass Enable
This bit controls PWR2 pin bypass mode which allows the PWR2 pin output value to be set directly. When bypass mode is enabled, the Trigger bits (REG[0230h] bits 1-0) and the Timing Delay bits (REG[0234] ~ REG[0238h]) have no effect.
When this bit = 0b, PWR2 pin bypass mode is disabled.
When this bit = 1b, PWR2 pin bypass mode is enabled and the PWR2 pin output is set to the value specified by the PWR2 Pin Bypass Value, REG[0232h] bit 3.

bit 10 PWR1 Pin Bypass Enable
This bit controls PWR1 pin bypass mode which allows the PWR1 pin output value to be set directly. When bypass mode is enabled, the Trigger bits (REG[0230h] bits 1-0) and the Timing Delay bits (REG[0234] ~ REG[0238h]) have no effect.
When this bit = 0b, PWR1 pin bypass mode is disabled.
When this bit = 1b, PWR1 pin bypass mode is enabled and the PWR1 pin output is set to the value specified by the PWR1 Pin Bypass Value, REG[0232h] bit 2.

bit 9 PWR0 Pin Bypass Enable
This bit controls PWR0 pin bypass mode which allows the PWR0 pin output value to be set directly. When bypass mode is enabled, the Trigger bits (REG[0230h] bits 1-0) and the Timing Delay bits (REG[0234] ~ REG[0238h]) have no effect.
When this bit = 0b, PWR0 pin bypass mode is disabled.
When this bit = 1b, PWR0 pin bypass mode is enabled and the PWR0 pin output is set to the value specified by the PWR0 Pin Bypass Value, REG[0232h] bit 1.

bit 8 PWRCOM Pin Bypass Enable
This bit controls PWRCOM pin bypass mode which allows the PWRCOM pin output value to be set directly. When bypass mode is enabled, the Trigger bits (REG[0230h] bits 1-0) and the Timing Delay bits (REG[0234] ~ REG[0238h]) have no effect.
When this bit = 0b, PWRCOM pin bypass mode is disabled.
When this bit = 1b, PWRCOM pin bypass mode is enabled and the PWRCOM pin output is set to the value specified by the PWRCOM Pin Bypass Value, REG[0232h] bit 0.

Note
If 3-Wire is selected for Power Line Management (REG[0020h] bit 0 = 1b), this bit controls the PWRCOM pin as well as the DAPWRALL pin.

bit 4 PWR3 Pin Bypass Value
When the PWR3 Pin Bypass Enable bit is set (REG[0232h] bit 12 = 1b), this bit specifies the value that is output on the PWR3 pin.
When this bit = 0b, a 0 is output on the PWR3 pin (low).
When this bit = 1b, a 1 is output on the PWR3 pin (high).

bit 3 PWR2 Pin Bypass Value
When the PWR2 Pin Bypass Enable bit is set (REG[0232h] bit 11 = 1b), this bit specifies the value that is output on the PWR2 pin.
When this bit = 0b, a 0 is output on the PWR2 pin (low).
When this bit = 1b, a 1 is output on the PWR2 pin (high).

bit 2 PWR1 Pin Bypass Value
When the PWR1 Pin Bypass Enable bit is set (REG[0232h] bit 10 = 1b), this bit specifies the value that is output on the PWR1 pin.
When this bit = 0b, a 0 is output on the PWR1 pin (low).
When this bit = 1b, a 1 is output on the PWR1 pin (high).

bit 1 PWR0 Pin Bypass Value
When the PWR0 Pin Bypass Enable bit is set (REG[0232h] bit 9 = 1b), this bit specifies the value that is output on the PWR0 pin.
When this bit = 0b, a 0 is output on the PWR0 pin (low).
When this bit = 1b, a 1 is output on the PWR0 pin (high).

bit 0 PWRCOM Pin Bypass Value
When the PWRCOM Pin Bypass Enable bit is set (REG[0232h] bit 8 = 1b), this bit specifies the value that is output on the PWRCOM pin.
When this bit = 0b, a 0 is output on the PWRCOM pin (low).
When this bit = 1b, a 1 is output on the PWRCOM pin (high).

Note
If 3-Wire is selected for Power Line Management (REG[0020h] bit 0 = 1b), this bit controls the PWRCOM pin as well as the DAPWRALL pin.

REG[0234h] Power Pin Timing Delay 0-1 Register
Default = 0000h Read/Write

n/a				Power Pin Timing Delay 0-1 bits 11-8			
15	14	13	12	11	10	9	8
Power Pin Timing Delay 0-1 bits 7-0							
7	6	5	4	3	2	1	0

bits 11-0 Power Pin Timing Delay 0-1 bits [11:0]
These bits specify the delay timing between PWR0 pin and PWR1 pin changes. For timing details, refer to 6.6.1, “Power Pin Transition Sequence for PWR[3:0]” on page 48.
Delay time = (REG[0234h] bits 11-0 + 1) x 16

Note
These bits must not be changed when the Power Cycle is busy, REG[0230h] bit 7 = 1b.

REG[0236h] Power Pin Timing Delay 1-2 Register
Default = 0000h Read/Write

n/a				Power Pin Timing Delay 1-2 bits 11-8			
15	14	13	12	11	10	9	8
Power Pin Timing Delay 1-2 bits 7-0							
7	6	5	4	3	2	1	0

bits 11-0 Power Pin Timing Delay 1-2 bits [11:0]
These bits specify the delay timing between PWR1 pin and PWR2 pin changes. For timing details, refer to 6.6.1, “Power Pin Transition Sequence for PWR[3:0]” on page 48.
Delay time = (REG[0236h] bits 11-0 + 1) x 16

Note
These bits must not be changed when the Power Cycle is busy, REG[0230h] bit 7 = 1b.

REG[0238h] Power Pin Timing Delay 2-3 Register
Default = 0000h Read/Write

n/a				Power Pin Timing Delay 2-3 bits 11-8			
15	14	13	12	11	10	9	8
Power Pin Timing Delay 2-3 bits 7-0							
7	6	5	4	3	2	1	0

bits 11-0 Power Pin Timing Delay 2-3 bits [11:0]
These bits specify the delay timing between PWR2 pin and PWR3 pin changes. For timing details, refer to 6.6.1, “Power Pin Transition Sequence for PWR[3:0]” on page 48.
Delay time = (REG[0238h] bits 11-0 + 1) x 16

Note
These bits must not be changed when the Power Cycle is busy, REG[0230h] bit 7 = 1b.

A.3.10 Interrupt Configuration Registers

REG[0240h] Interrupt Raw Status Register
Default = 0000h Read/Write

n/a							
15	14	13	12	11	10	9	8
SDRAM Self Refresh Enter/Exit Interrupt Raw Status	Host Memory Read/Write FIFO Error Interrupt Raw Status	Power Management Controller Interrupt Raw Status	3-Wire Chip Interrupt Raw Status	GPIO Interrupt Raw Status	SDRAM Access Complete Interrupt Raw Status	Display Engine Interrupt Raw Status	SDRAM Initialization Complete Interrupt Raw Status
7	6	5	4	3	2	1	0

bit 7 SDRAM Self Refresh Enter/Exit Interrupt Raw Status

This bit indicates the raw status of the SDRAM Self Refresh Enter/Exit Interrupt and is not masked by the SDRAM Self Refresh Enter/Exit Interrupt Enable bit, REG[0244h] bit 7.

When this bit = 0b, a SDRAM Self Refresh Enter/Exit Interrupt has not occurred.

When this bit = 1b, a SDRAM Self Refresh Enter/Exit Interrupt has occurred.

To clear this status bit, write a 1b to either this bit or REG[0242h] bit 7.

bit 6 Host Memory Read/Write FIFO Error Interrupt Raw Status

This bit indicates the raw status of the Host Memory Read/Write FIFO Error Interrupt and is not masked by the Host Memory Read/Write FIFO Error Interrupt Enable bit, REG[0244h] bit 6.

When this bit = 0b, a Host Memory Read/Write FIFO Error Interrupt has not occurred.

When this bit = 1b, a Host Memory Read/Write FIFO Error Interrupt has occurred.

To clear this status bit, write a 1b to either this bit or REG[0242h] bit 6.

Note

Host memory accesses must **stop immediately** if this interrupt goes high and must not be continued until the host memory interface is no longer busy, REG[0140h] bit 12 = 0b. This interrupt will not occur if data is not written to or read from the Host Memory Access Port (REG[0154h]) when the Host Memory Interface is busy, REG[0140h] bit 12 = 1b.

bit 5 Power Management Controller Interrupt Raw Status

This bit indicates the raw status of the Power Management Controller Interrupt and is not masked by the Power Management Controller Interrupt Enable bit, REG[0244h] bit 5.

When this bit = 0b, a Power Management Controller Interrupt has not occurred.

When this bit = 1b, a Power Management Controller Interrupt has occurred.

To clear this status bit, write a 1b to either this bit or REG[0242h] bit 5.

bit 4 3-Wire Chip Interrupt Raw Status

This bit indicates the raw status of the 3-Wire Chip Interrupt and is not masked by the 3-Wire Chip Interrupt Enable bit, REG[0244h] bit 4.

When this bit = 0b, a 3-Wire Chip Interrupt has not occurred.

When this bit = 1b, a 3-Wire Chip Interrupt has occurred.

To clear this status bit, write a 1b to either this bit or REG[0242h] bit 4.

bit 3 GPIO Interrupt Raw Status

This bit indicates the raw status of the GPIO Interrupt and is not masked by the GPIO Interrupt Enable bit, REG[0244h] bit 3. For configuration and status of each individual GPIO, see REG[0254h] and REG[0256h].
When this bit = 0b, a GPIO Interrupt has not occurred.
When this bit = 1b, a GPIO Interrupt has occurred.

To clear this status bit, write a 1b to the appropriate GPIO[1:0] Negative/Positive Interrupt Status bit in REG[0256h].

bit 2 SDRAM Access Complete Interrupt Raw Status

This bit indicates the raw status of the host memory transfer to or from the SDRAM. Once the SDRAM access is complete, this interrupt will go high. This bit is not masked by the SDRAM Access Complete Interrupt Enable bit, REG[0244h] bit 2.
When this bit = 0b, a SDRAM Access Complete Interrupt has not occurred.
When this bit = 1b, a SDRAM Access Complete Interrupt has occurred.

To clear this status bit, write a 1b to either this bit or REG[0242h] bit 2.

Note

For Raw Memory Reads, the host should read the remaining data buffered by the FIFO after this interrupt goes high.

bit 1 Display Engine Interrupt Raw Status

This bit indicates the raw status of the Display Engine Interrupt which occurs when one of the interrupts in REG[033Ah] or REG[033Ch] is triggered. This bit is not masked by the Display Engine Interrupt Enable bit, REG[0244h] bit 1.
When this bit = 0b, a Display Engine Interrupt has not occurred.
When this bit = 1b, a Display Engine Interrupt has occurred.

To clear this status bit, clear the triggering interrupt in REG[033Ah] or REG[033Ch].

bit 0 SDRAM Initialization Complete Interrupt Raw Status

This bit indicates the raw status of the SDRAM Initialization Complete Interrupt and is not masked by the SDRAM Initialization Complete Interrupt Enable bit, REG[0244h] bit 0.
When this bit = 0b, a SDRAM Initialization Complete Interrupt has not occurred.
When this bit = 1b, a SDRAM Initialization Complete Interrupt has occurred.

To clear this status bit, write a 1b to either this bit or REG[0242h] bit 0.

Note

This bit can be used only if the SDRAM is not already initialized, REG[0102h] bit 8 = 1b.

REG[0242h] Interrupt Masked Status Register
Default = 0000h Read/Write

n/a							
15	14	13	12	11	10	9	8
SDRAM Self Refresh Enter/Exit Interrupt Masked Status	Host Memory Read/Write FIFO Error Interrupt Masked Status	Power Management Controller Interrupt Masked Status	3-Wire Chip Interrupt Masked Status	GPIO Interrupt Masked Status	SDRAM Access Complete Interrupt Masked Status	Display Engine Interrupt Masked Status	SDRAM Initialization Complete Interrupt Masked Status
7	6	5	4	3	2	1	0

bit 7 SDRAM Self Refresh Enter/Exit Interrupt Masked Status
This bit indicates the masked status of the SDRAM Self Refresh Enter/Exit Interrupt (see REG[0244h] bit 7).
When this bit = 0b, a SDRAM Self Refresh Enter/Exit Interrupt has not occurred.
When this bit = 1b, a SDRAM Self Refresh Enter/Exit Interrupt has occurred.

To clear this status bit, write a 1b to either this bit or REG[0240h] bit 7.

bit 6 Host Memory Read/Write FIFO Error Interrupt Masked Status
This bit indicates the masked status of the Host Memory Read/Write FIFO Error Interrupt (see REG[0244h] bit 6).
When this bit = 0b, a Host Memory Read/Write FIFO Error Interrupt has not occurred.
When this bit = 1b, a Host Memory Read/Write FIFO Error Interrupt has occurred.

To clear this status bit, write a 1b to either this bit or REG[0240h] bit 6.

Note
Host memory accesses must **stop immediately** if this interrupt goes high and must not be continued until the host memory interface is no longer busy, REG[0140h] bit 12 = 0b. This interrupt will not occur if data is not written to or read from the Host Memory Access Port (REG[0154h]) when the Host Memory Interface is busy, REG[0140h] bit 12 = 1b.

bit 5 Power Management Controller Interrupt Masked Status
This bit indicates the masked status of the Power Management Controller Interrupt (see REG[0244h] bit 5).
When this bit = 0b, a Power Management Controller Interrupt has not occurred.
When this bit = 1b, a Power Management Controller Interrupt has occurred.

To clear this status bit, write a 1b to either this bit or REG[0240h] bit 5.

bit 4 3-Wire Chip Interrupt Masked Status
This bit indicates the masked status of the 3-Wire Chip Interrupt (see REG[0244h] bit 4).
When this bit = 0b, a 3-Wire Chip Interrupt has not occurred.
When this bit = 1b, a 3-Wire Chip Interrupt has occurred.

To clear this status bit, write a 1b to either this bit or REG[0240h] bit 4.

bit 3 GPIO Interrupt Masked Status
This bit indicates the masked status of the GPIO Interrupt (see REG[0244h] bit 3). For configuration and status of each individual GPIO, see REG[0254h] and REG[0256h].
When this bit = 0b, a GPIO Interrupt has not occurred.
When this bit = 1b, a GPIO Interrupt has occurred.

To clear this status bit, write a 1b to the appropriate GPIO[1:0] Negative/Positive Interrupt Status bit in REG[0256h].

bit 2 SDRAM Access Complete Interrupt Masked Status
This bit indicates the masked status of the host memory transfer to or from the SDRAM (see REG[0244h] bit 2). Once the SDRAM access is complete, this interrupt will go high.
When this bit = 0b, a SDRAM Access Complete Interrupt has not occurred.
When this bit = 1b, a SDRAM Access Complete Interrupt has occurred.

To clear this status bit, write a 1b to either this bit or REG[0240h] bit 2.

Note
For Raw Memory Reads, the host should read the remaining data buffered by the FIFO after this interrupt goes high.

bit 1 Display Engine Interrupt Masked Status
This bit indicates the masked status of the Display Engine Interrupt (see REG[0244h] bit 1) which occurs when one of the interrupts in REG[033Ah] or REG[033Ch] is triggered.
When this bit = 0b, a Display Engine Interrupt has not occurred.
When this bit = 1b, a Display Engine Interrupt has occurred.

To clear this status bit, clear the triggering interrupt in REG[033Ah] or REG[033Ch].

bit 0 SDRAM Initialization Complete Interrupt Masked Status
This bit indicates the masked status of the SDRAM Initialization Complete Interrupt (see REG[0244h] bit 0).
When this bit = 0b, a SDRAM Initialization Complete Interrupt has not occurred.
When this bit = 1b, a SDRAM Initialization Complete Interrupt has occurred.

To clear this status bit, write a 1b to either this bit or REG[0240h] bit 0.

Note
This bit can be used only if the SDRAM is not already initialized, REG[0102h] bit 8 = 1b.

REG[0244h] Interrupt Control Register
Default = 0000h Read/Write

n/a							
15	14	13	12	11	10	9	8
SDRAM Self Refresh Enter/Exit Interrupt Enable	Host Memory Read/Write FIFO Error Interrupt Enable	Power Management Controller Interrupt Enable	3-Wire Chip Interrupt Enable	GPIO Interrupt Enable	SDRAM Access Complete Interrupt Enable	Display Engine Interrupt Enable	SDRAM Initialization Complete Interrupt Enable
7	6	5	4	3	2	1	0

bit 7 SDRAM Self Refresh Enter/Exit Interrupt Enable
This bit controls whether the SDRAM Self Refresh Enter/Exit Interrupt causes an interrupt request on the HIRQ pin. The status of this interrupt can be determined by reading REG[0240h] bit 7 (unmasked) or REG[0242h] bit 7 (masked).
When this bit = 0b, the interrupt is disabled.
When this bit = 1b, the interrupt is enabled.

bit 6 Host Memory Read/Write FIFO Error Interrupt Enable
This bit controls whether the Host Memory Read/Write FIFO Error Interrupt causes an interrupt request on the HIRQ pin. The status of this interrupt can be determined by reading REG[0240h] bit 6 (unmasked) or REG[0242h] bit 6 (masked).
When this bit = 0b, the interrupt is disabled.
When this bit = 1b, the interrupt is enabled

bit 5 Power Management Controller Interrupt Enable
This bit controls whether the Power Management Controller Interrupt causes an interrupt request on the HIRQ pin. The status of this interrupt can be determined by reading REG[0240h] bit 5 (unmasked) or REG[0242h] bit 5 (masked).
When this bit = 0b, the interrupt is disabled.
When this bit = 1b, the interrupt is enabled.

bit 4 3-Wire Chip Interrupt Enable
This bit controls whether the 3-Wire Chip Interrupt causes an interrupt request on the HIRQ pin. The status of this interrupt can be determined by reading REG[0240h] bit 4 (unmasked) or REG[0242h] bit 4 (masked).
When this bit = 0b, the interrupt is disabled.
When this bit = 1b, the interrupt is enabled.

bit 3 GPIO Interrupt Enable
This bit controls whether the GPIO Interrupt causes an interrupt request on the HIRQ pin. The status of this interrupt can be determined by reading REG[0240h] bit 3 (unmasked) or REG[0242h] bit 3 (masked).
When this bit = 0b, the interrupt is disabled.
When this bit = 1b, the interrupt is enabled.

bit 2 SDRAM Access Complete Interrupt Enable
This bit controls whether the SDRAM Access Complete Interrupt causes an interrupt request on the HIRQ pin. The status of this interrupt can be determined by reading REG[0240h] bit 2 (unmasked) or REG[0242h] bit 2 (masked).
When this bit = 0b, the interrupt is disabled.
When this bit = 1b, the interrupt is enabled.

bit 1 Display Engine Interrupt Enable
This bit controls whether the Display Engine Interrupt causes an interrupt request on the HIRQ pin. The status of this interrupt can be determined by reading REG[0240h] bit 1 (unmasked) or REG[0242h] bit 1 (masked).
When this bit = 0b, the interrupt is disabled.
When this bit = 1b, the interrupt is enabled.

bit 0 SDRAM Initialization Complete Interrupt Enable
This bit controls whether the SDRAM Initialization Complete Interrupt causes an interrupt request on the HIRQ pin. The status of this interrupt can be determined by reading REG[0240h] bit 0 (unmasked) or REG[0242h] bit 0 (masked).
When this bit = 0b, the interrupt is disabled.
When this bit = 1b, the interrupt is enabled.

Note
This bit can be used only if the SDRAM is not already initialized, REG[0102h] bit 8 = 1b.

A.3.11 GPIO Control Registers

REG[0250h] GPIO Configuration Register
Default = 0000h — Read/Write

15	14	13	12	11	10	9	8
n/a						GPIO1 Pull-down Control	GPIO0 Pull-down Control
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
n/a						GPIO1 Configuration	GPIO0 Configuration

bits 9-8 GPIO[1:0] Pull-down Control
All GPIO pins have internal pull-down resistors. These bits control the state of the pull-down resistor for each GPIOx pin.
When the bit = 0b, the pull-down resistor for the corresponding GPIOx pin is inactive. (default)
When the bit = 1b, the pull-down resistor for the corresponding GPIO pin is active.

bits 1-0 GPIO[1:0] Configuration
These bits configure each individual GPIO pin between an input or an output.
When this bit = 0b, the corresponding GPIO pin is configured as an input pin. (default)
When this bit = 1b, the corresponding GPIO pin is configured as an output pin.

REG[0252h] GPIO Status/Control Register
Default = 0000h — Read/Write

15	14	13	12	11	10	9	8
n/a						GPIO1 Input Status (RO)	GPIO0 Input Status (RO)
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
n/a						GPIO1 Data Output Control	GPIO0 Data Output Control

bits 9-8 GPIO[1:0] Input Status (Read Only)
When GPIOx is configured as an input (see REG[0250h] bits 1-0), a read from this bit returns the state of the corresponding GPIOx pin.
When this bit = 0b, the GPIOx pin is 0 (low).
When this bit = 1b, the GPIOx pin is 1 (high).

bits 1-0 GPIO[1:0] Data Output Control
When GPIOx is configured as an output (see REG[0250h] bits 1-0), a write to this bit drives the output state of the corresponding GPIOx pin.
When this bit = 0b, the corresponding GPIOx pin is driven to 0 (low). (default)
When this bit = 1b, the corresponding GPIOx pin is driven to 1 (high).

REG[0254h] GPIO Interrupt Enable Register
Default = 0000h — Read/Write

15	14	13	12	11	10	9	8
n/a						GPIO1 Negative Edge Interrupt Enable	GPIO0 Negative Edge Interrupt Enable
7	6	5	4	3	2	1	0
n/a						GPIO1 Positive Edge Interrupt Enable	GPIO0 Positive Edge Interrupt Enable

bits 9-8 GPIO[1:0] Negative Edge Interrupt Enable
These bits control whether the corresponding GPIOx interrupt (see REG[0256h]) is triggered on the negative edge (when the GPIOx pin changes from 1 to 0).
When this bit = 0b, the corresponding GPIOx interrupt is not triggered on the negative edge. (default)
When this bit = 1b, the corresponding GPIOx interrupt is triggered on the negative edge.

bits 1-0 GPIO[1:0] Positive Edge Interrupt Enable
These bits control whether the corresponding GPIOx interrupt (see REG[0256h]) is triggered on the positive edge (when the GPIOx pin changes from 0 to 1).
When this bit = 0b, the corresponding GPIOx interrupt is not triggered on the positive edge. (default)
When this bit = 1b, the corresponding GPIOx interrupt is triggered on the positive edge.

REG[0256h] GPIO Interrupt Status Register
Default = 0000h — Read/Write

15	14	13	12	11	10	9	8
n/a						GPIO1 Negative Edge Interrupt Status	GPIO0 Negative Edge Interrupt Status
7	6	5	4	3	2	1	0
n/a						GPIO1 Positive Edge Interrupt Status	GPIO0 Positive Edge Interrupt Status

bits 9-8 GPIO[1:0] Negative Edge Interrupt Status
These bits indicate the status of the corresponding GPIOx Negative Edge Interrupt.
When this bit = 0b, a Negative Edge Interrupt has not occurred. (default)
When this bit = 1b, a Negative Edge Interrupt has occurred.

To clear this status bit, write a 1b to this bit.

bits 1-0 GPIO[1:0] Positive Edge Interrupt Status
These bits indicate the status of the corresponding GPIOx Positive Edge Interrupt.
When this bit = 0b, a Positive Edge Interrupt has not occurred. (default)
When this bit = 1b, a Positive Edge Interrupt has occurred.

To clear this status bit, write a 1b to this bit.

A.3.12 Command RAM Controller Registers

REG[0290h] Command RAM Controller Configuration Register
Default = 0000h — Read/Write

15	14	13	12	11	10	9	8
n/a							
7	6	5	4	3	2	1	0
n/a							Command RAM Access Read/Write Select

bit 0 — Command RAM Access Read/Write Select
This bit selects whether the Command RAM is read from or written to when the Host accesses the Command RAM Access Port, REG[0294h].
When this bit = 0b, a write access is selected.
When this bit = 1b, a read access is selected.

REG[0292h] Command RAM Controller Address Register
Default = 0000h — Read/Write

15	14	13	12	11	10	9	8
n/a					Command RAM Address Pointer bits 10-8		
7	6	5	4	3	2	1	0
Command RAM Address Pointer bits 7-0							

bits 10-0 — Command RAM Address Pointer bits [10:0]
These bits specify the byte address in the Command RAM where data is read from or written to for each access to the Command RAM Access Port, REG[0294h]. After every access to REG[0294h], this register is auto incremented by +2.

REG[0294h] Command RAM Controller Access Port Register
Default = 0000h — Read/Write

15	14	13	12	11	10	9	8
Command RAM Access Port bits 15-8							
7	6	5	4	3	2	1	0
Command RAM Access Port bits 7-0							

bits 15-0 — Command RAM Access Port bits [15:0]
These bits are the access port for the Command RAM.
For read accesses (REG[0290h] bit 0 = 0b), data is retrieved from the Command RAM address specified by REG[0292h] and can be read from these bits on the next read access to this register.
For write accesses (REG[0290h] bit 0 = 1b), these bits store the data that is written to the Command RAM address specified by REG[0292h].

REG[02A0h] through REG[02A2h] are Reserved

These registers are Reserved and should not be written.

A.3.13 Display Engine: Display Timing Configuration

REG[0300h] Frame Data Length Register
Default = 0258h Read/Write

15	14	13	12	11	10	9	8
n/a			Frame Data Length bits 12-8				
Frame Data Length bits 7-0							
7	6	5	4	3	2	1	0

bits 12-0 Frame Data Length bits [12:0]
These bits specify the frame data length, in lines.
Frame data length = REG[0300h] bits 12-0

Note
For a line data length (horizontal display size, see REG[0306h]) greater than 2048, only raw memory writes are supported.

REG[0302h] Frame Sync Length Register
Default = 0004h Read/Write

15	14	13	12	11	10	9	8
n/a							
Frame Sync Length bits 7-0							
7	6	5	4	3	2	1	0

bits 7-0 Frame Sync Length bits [7:0]
These bits specify the frame sync length, in lines.
Frame sync length = REG[0302h] bits 7-0

REG[0304h] Frame Begin/End Length Register
Default = 0A04h Read/Write

15	14	13	12	11	10	9	8
Frame End Length bits 7-0							
Frame Begin Length bits 7-0							
7	6	5	4	3	2	1	0

bits 15-8 Frame End Length bits [7:0]
These bits specify the frame end length, in lines.
Frame end length = REG[0304h] bits 15-8 + 1

Note
These bits must be programmed such that the following formula is valid.
REG[0304h] bits 15-8 ≥ 1

bits 7-0 Frame Begin Length bits [7:0]
These bits specify the frame begin length, in lines.
Frame begin length = REG[0304h] bits 7-0

Note
These bits must be programmed according to the gate driver specification. For the Sharp LH1692, these bits must be set to 4h. For other generic Gate drivers, these bits must be set to 0h.

REG[0306h] Line Data Length Register
Default = 0320h Read/Write

n/a			Line Data Length bits 12-8				
15	14	13	12	11	10	9	8
Line Data Length bits 7-0							
7	6	5	4	3	2	1	0

bits 12-0 Line Data Length bits [12:0]
These bits specify the line data length, in pixels.
These bits, in combination with the Source Driver Output Size bits (REG[030Ch] bits 7-0), define the data output time, including the padding pixels needed if the line data length is not an integer multiple of the source driver output size. For timing details, refer to 6.5.2, “Interpreted Source Driver Timings” on page 39.

Note

1. These bits must be programmed to a multiple of 16, and must not be programmed to a value larger than the Source Driver Output Size x 9 (see REG[030Ch] bits 7-0).
2. For a line data length (horizontal display size, see REG[0306h]) greater than 2048, only raw memory writes are supported.

REG[0308h] Line Sync Length Register
Default = 000Ah Read/Write

n/a							
15	14	13	12	11	10	9	8
Line Sync Length bits 7-0							
7	6	5	4	3	2	1	0

bits 7-0 Line Sync Length bits [7:0]
These bits specify the line sync length, in SDCLK cycles.

Note

These bits must be programmed such that the following formulae are valid.
REG[0308h] bits 7-0 ≥ 1 (for 4 pixels per clock cycle)
REG[0308h] bits 7-0 ≥ 2 (for 8 pixels per clock cycle)

REG[030Ah] Line Begin/End Length Register
Default = 6404h Read/Write

Line End Length bits 7-0							
15	14	13	12	11	10	9	8
Line Begin Length bits 7-0							
7	6	5	4	3	2	1	0

bits 15-8 Line End Length bits [7:0]
These bits specify the line end length, in SCLK cycles.

For 4 pixels per clock cycle (REG[030Ch] bit 11 = 0b),
Line end length
= (REG[030Ah] bits 15-8 - 1) x SDCLK period - Padded Data Output Time - PCLK period
For 8 pixels per clock cycle (REG[030Ch] bit 11 = 1b),
Line end length
= ((REG[030Ah] bits 15-8 ÷ 2) - 1) x SDCLK period - Padded Data Output Time - PCLK period

Note
These bits must be programmed such that the following formulae are valid.
Line end length ≥ 0
REG[030Ah] bits 15-8 ≥ 2 (for 4 pixels per clock cycle)
REG[030Ah] bits 15-8 ≥ 4 (for 8 pixels per clock cycle)

bits 7-0 Line Begin Length bits [7:0]
These bits specify the line begin length, in SDCLK cycles.

For 4 pixels per clock cycle (REG[030Ch] bit 11 = 0b),
Line begin length = REG[030Ah] bits 7-0
For 8 pixels per clock cycle (REG[030Ch] bit 11 = 1b),
Line begin length = REG[030Ah] bits 7-0 ÷ 2

A.3.14 Display Engine: Driver Configurations

REG[030Ch] Source Driver Configuration Register
Default = 0064h — Read/Write

Source Driver Chip Enable Start bits 3-0				Source Driver Pixel Output Count Select	Source Driver Chip Enable Reverse	Source Driver Output Reverse	Source Driver Shift
15	14	13	12	11	10	9	8
Source Driver Output Size Select bits 7-0							
7	6	5	4	3	2	1	0

bits 15-12 Source Driver Chip Enable Start bits [3:0]
These bits determine the number of the driver chip to start driving. The Source Driver Chip Enable Reverse bit (REG[030Ch] bit 10) can be used to reverse the chip enable sequence. For an example, see the following table.

Table 21-21: Example of Chip Enable Start + Chip Enable Reverse (ChipSize = 268, Line Size = 800)

REG[030Ch] bit 10	REG[030Ch] bits 15-12	Chip Enable Sequence
0b	0000b	Chip0 -> Chip1 -> Chip2
	0001b	Chip1 -> Chip2 -> Chip0
	0010b	Chip2 -> Chip0 -> Chip1
	0011b ~ 1111b	Reserved
1b	0000b	Chip0 -> Chip2 -> Chip1
	0001b	Chip1 -> Chip0 -> Chip2
	0010b	Chip2 -> Chip1-> Chip0
	0011b ~ 1111b	Reserved

Note
1. These bits must not be set greater than the number of SDCE_L lines in use.
2. For multi-panel implementations, refer to 12.6, “Multi-Panel Support” on page 110.

bit 11 Source Driver Pixel Output Count Select
This bit selects the number of parallel pixels output per Source Driver clock.
When this bit = 0b, the source driver outputs 4 pixels per clock.
When this bit = 1b, the source driver outputs 8 pixels per clock.

bit 10 Source Driver Chip Enable Reverse
This bit configures the enable sequence for multiple chip selects. The number of chip selects is determined by the Line Data Length bits (REG[0306h] bits 12-0) and the Source Driver Output Size Select bits (REG[030Ch] bits 6-0). Using these bits with the Source Driver Chip Enable Start bit provides full configurability of the count down sequence.
When this bit = 0b, the source driver chip enable sequence is not reversed.
When this bit = 1b, the source driver chip enable sequence is reversed.

bit 9 Source Driver Output Reverse

This bit selects the parallel pixels output arrangement.

Table 21-22: Source Driver Output Reverse Function

REG[030Ch] bit 11	Pixels Arrangement in Little Endian	REG[030Ch] bit 9	Parallel Output to Source Driver
0	P3,P2,P1,P0	0	P3,P2,P1,P0
0	P3,P2,P1,P0	1	P0,P1,P2,P3
1	P7,P6,P5,P4,P3,P2,P1,P0	0	P7,P6,P5,P4,P3,P2,P1,P0
1	P7,P6,P5,P4,P3,P2,P1,P0	1	P0,P1,P2,P3,P4,P5,P6,P7

Note

If 8 pixel per clock and double data rate is used (REG[030Ch] bit 11 = 1b and REG[030Eh] bit 10 = 1b), this bit must be set to 0b.

bit 8 Source Driver Shift

This bit determines how the source driver shifts the Serial to Parallel data.

When this bit = 0b, the serial to parallel data is shifted from Left to Right. The first data input is shifted from the last source driver output to the first source driver output (i.e. for 268 size, 268 -> 1). This means the first data accepted by the source driver will appear on the first line of the source driver.

When this bit = 1b, the serial to parallel data is shifted from Right to Left. The first data input is shifted from the first source driver output to the last source driver output (i.e. for 268 size, 1 -> 268). This means the first data accepted by the source driver will appear on the last line of the source driver.

bits 7-0 Source Driver Output Size Select bits [7:0]

These bits select the source driver output size per chip.

REG[030Ch] bits 7-0 = value in pixels ÷ 4

For example, the default value of 64h results in the following source driver output size.

REG[030Ch] bits 7-0 = 400 ÷ 4
= 100
= 64h

Note

For 4 pixel per clock source driver output (REG[030Ch] bit 11 = 0b), these bits must be set to a value greater than 0. For 8 pixels per clock source driver output (REG[030Ch] bit 11 = 1b), these bits must be set to an even value greater than 1.

REG[030Eh] Gate Driver Configuration Register
Default = 0000h — Read/Write

Source Driver SDOED Delay bits 4-0					Source Driver Double Data Rate Enable	Source Driver Swap Padding Pixels	Source Driver Early SDOE Assert Disable
15	14	13	12	11	10	9	8
Source Driver SDOEX Delay bits 4-0					n/a	Gate Driver Right/Left Select	Gate Driver Start Pulse Polarity
7	6	5	4	3	2	1	0

bits 15-11 Source Driver SDOED Delay bits [4:0]
These bits are only used for 8 pixel per clock output with double data rate enabled, REG[030Ch] bit 11 = 1b and REG[030Eh] bit 10 = 1b.
These bits specify the SDOED delay from SDLE, in SDCLKs.

Note
These bits must be programmed such that the following formula is valid.
REG[030Eh] bits 15-11 > 0

bit 10 Source Driver Double Data Rate Enable
This bit is used when the source driver pixel output count is set to 8 pixels.
When this bit = 0b, 8 pixels are output per SDCLK.
When this bit = 1b, the data rate is doubled and 4 pixels are output per SDCLK edge (positive and negative edges).

bit 9 Source Driver Swap Padding Pixels
This bit is used in combination with the Source Driver Shift Right bit (REG[030Ch] bit 8) and causes pixels padding whenever the Source Driver chip contains extra unused/non-display pixels.

Table 21-23: Source Driver Padding Pixels Position

REG[030Eh] bit 9	REG[030Ch] bit 8	Padding Data Location
0b	0b	Extra Pixels will be padded at the end of the Last Chip
0b	1b	Extra Pixels will be padded at the beginning of the First Chip
1b	0b	Extra Pixels will be padded at the beginning of the First Chip
1b	1b	Extra Pixels will be padded at the end of the Last Chip

bit 8 Source Driver Early SDOE Assert Disable
This bit determines whether SDOE is asserted 1 line early before SDLE in normal operation (for non-Micronix source drivers).
When this bit = 0b, Source Driver Early SDOE Assert is enabled.
When this bit = 1b, Source Driver Early SDOE Assert is disabled.

bits 7-3 Source Driver SDOEX Delay bits [4:0]
These bits are only used for 8 pixel per clock output with double data rate enabled, REG[030Ch] bit 11 = 1b and REG[030Eh] bit 10 = 1b.
These bits specify the SDOEX delay from SDLE, in SDCLKs.

Note
These bits must be programmed such that the following formula is valid.
REG[030Eh] bits 7-3 > 0

bit 1 Gate Driver Right/Left Select
This bit selects the gate driver GDRL pin output.
When this bit = 0b, the Gate Driver GDRL pin output is left.
When this bit = 1b, the Gate Driver GDRL pin output is right.

bit 0 Gate Driver Start Pulse Polarity
This bit controls the gate driver start pulse polarity.
When this bit = 0b, the polarity is negative.
When this bit = 1b, the polarity is positive.

A.3.15 Display Engine: Memory Region Configuration Registers

REG[0310h] Image Buffer Start Address Register 0
Default = 0000h — Read/Write

15	14	13	12	11	10	9	8
Image Buffer Start Address bits 15-8							
7	6	5	4	3	2	1	0
Image Buffer Start Address bits 7-0 (bits 2-0 are always 000b)							

REG[0312h] Image Buffer Start Address Register 1
Default = 0080h — Read/Write

15	14	13	12	11	10	9	8
n/a						Image Buffer Start Address bits 25-24	
7	6	5	4	3	2	1	0
Image Buffer Start Address bits 23-16							

REG[0312h] bits 9-0
REG[0310h] bits 15-0 Image Buffer Start Address bits [25:0]
These bits specify the Image Buffer start address in SDRAM byte address space. The Image Buffer start address must be 64-bit aligned (writing to bits 2-0 has no effect and bits 2-0 always return 000b).

REG[0314h] Update Buffer Start Address Register 0
Default = 0000h — Read/Write

15	14	13	12	11	10	9	8
Update Buffer Start Address bits 15-8							
7	6	5	4	3	2	1	0
Update Buffer Start Address bits 7-0 (bits 2-0 are always 000b)							

REG[0316h] Update Buffer Start Address Register 1
Default = 0000h — Read/Write

15	14	13	12	11	10	9	8
n/a						Update Buffer Start Address bits 25-24	
7	6	5	4	3	2	1	0
Update Buffer Start Address bits 23-16							

REG[0316h] bits 9-0
REG[0314h] bits 15-0 Update Buffer Start Address bits [25:0]
These bits specify the Update Buffer start address in SDRAM byte address space. The Update Buffer start address must be 64-bit aligned (writing to bits 2-0 has no effect and bits 2-0 always return 000b).

A.3.16 Display Engine: Component Control

REG[0320h] Temperature Device Select Register
Default = 0000h Read/Write

15	14	13	12	11	10	9	8
n/a							
7	6	5	4	3	2	1	0
n/a						Temperature Device Source Select	Temperature Auto Retrieval Disable

bit 1 Temperature Device Source Select
This bit selects between the I2C thermal sensor or the 3-wire Active Matrix Power Management IC for Temperature Sensing device. This bit must be set to 0b when the 3-wire Active Matrix Power Management IC is not present.
When this bit = 0b, the I2C thermal sensor is selected.
When this bit = 1b, the 3-wire Active Matrix Power Management IC is selected for power management.

bit 0 Temperature Auto Retrieval Disable
This bit determines whether the temperature is retrieved from the selected device (see bit 1) on every update frame operation.
When this bit = 0b, temperature retrieval is enabled. (default)
When this bit = 1b, temperature retrieval is disabled.

REG[0322h] Temperature Value Register
Default = 0000h Read/Write

15	14	13	12	11	10	9	8
n/a							
7	6	5	4	3	2	1	0
Temperature Value bits 7-0							

bits 7-0 Temperature Value bits [7:0]
These bits store the temperature value which will be used for Waveform retrieval on the next display update operation. When Temperature Auto Retrieval is enabled (REG[0320h] bit 0 = 0b), these bits are automatically updated on every frame update operation.

REG[0324h] is Reserved

This register is Reserved and should not be written.

REG[0326h] Border Configuration Register
Default = 0000h Read/Write

15	14	13	12	11	10	9	8
Reserved)							
7	6	5	4	3	2	1	0
Next Border Value bits 7-0							

bits 15-8 Reserved
The default value for these bits is 00h.

bits 7-0 Next Border Value bits [7:0]
These bits specify the Next Border Value requested. The most significant bits will be used according to the selected LUT index mode.

REG[0328h] is Reserved

This register is Reserved and should not be written.

REG[032Ah] Power Control Configuration Register
Default = 000Fh Read/Write

15	14	13	12	11	10	9	8
n/a							Voltage Control Byte Force Frame Wait
7	6	5	4	3	2	1	0
Voltage Control Byte Wait Select bits 3-0				Voltage Control Byte 3 Enable	Voltage Control Byte 2 Enable	Voltage Control Byte 1 Enable	Voltage Control Byte 0 Enable

These bits are only active when the Waveform data format is version 2 - voltage control format. This bits correspond to the Version 2 waveform data which contains an additional 4 bytes at the beginning of each temperature compensated waveform data.

bit 8 Voltage Control Byte Force Frame Wait
This bit forces the number of frames specified by REG[032Ah] bits 7-4 to be skipped before the next frame is displayed.

bits 7-4 Voltage Control Byte Wait Select bits [3:0]
When the value of a voltage control byte changes, these bits specify the number of frames that are skipped before the next frame is displayed.

bit 3 Voltage Control Byte 3 Enable
This bit controls Power Control programming.
When this bit = 0b, Voltage Control Byte 3 is disabled.
When this bit = 1b, Voltage Control Byte 3 is enabled.

bit 2 Voltage Control Byte 2 Enable
This bit controls Power Control VCOMS programming.
When this bit = 0b, Voltage Control Byte 2 is disabled.
When this bit = 1b, Voltage Control Byte 2 is enabled.

bit 1 Voltage Control Byte 1 Enable
This bit controls Power Control VEES/VCCS programming.
When this bit = 0b, Voltage Control Byte 1 is disabled.
When this bit = 1b, Voltage Control Byte 1 is enabled.

bit 0 Voltage Control Byte 0 Enable
This bit controls Power Control VNEGS/VPOSS programming.
When this bit = 0b, Voltage Control Byte 0 is disabled.
When this bit = 1b, Voltage Control Byte 0 is enabled.

REG[032Ch] General Configuration Register
Default = 0000h Read/Write

n/a					Area Coordinate End Size Select	Area Coordinate Rotation Select bits 1-0	
15	14	13	12	11	10	9	8
n/a		Reserved		n/a			
7	6	5	4	3	2	1	0

bit 10 Area Coordinate End Size Select
This bit selects whether REG[0344h] ~ REG[0346h] define the X/Y end coordinates of the area update or the horizontal/vertical size of the area update relative to the X/Y start position (REG[0340h] ~ REG[0342h]).
When this bit = 0b, REG[0344h] ~ REG[0346h] define the X/Y end coordinates for the area update.
When this bit = 1b, REG[0344h] ~ REG[0346h] define the horizontal/vertical size for the area update.

bits 9-8 Area Coordinate Rotation Select bits [1:0]
These bits select the rotation mode used to define the area update input coordinates (REG[0340h] ~ REG[0346h]).

Table 21-24 : Area Coordinate Rotation Selection

REG[032Ch] bits 9-8	Area Coordinate Rotation
00b	0°
01b	90°
10b	180°
11b	270°

Note
When Update Rectangle Mode bits is set to use the Host X/Y Start/End Positions (REG[0334h] bits 13-12 = 01b), these bits must be set to the same rotation as the Write Rotation Select bits, REG[0140h] bits 9-8.

bits 5-4 Reserved
The default value for these bits is 00b.

REG[032Eh] LUT Mask Register
Default = 0000h Read/Write

LUT 15 Mask	LUT 14 Mask	LUT 13 Mask	LUT 12 Mask	LUT 11 Mask	LUT 10 Mask	LUT 9 Mask	LUT 8 Mask
15	14	13	12	11	10	9	8
LUT 7 Mask	LUT 6 Mask	LUT 5 Mask	LUT 4 Mask	LUT 3 Mask	LUT 2 Mask	LUT 1 Mask	LUT 0 Mask
7	6	5	4	3	2	1	0

bits 15-0 LUT [15:0] Mask
These bits specify which LUTs (0-15) are included in the available status of the Masked LUT Status bit, REG[0338h] bit 6.
When this bit = 0b, the available status of LUTx is not included in REG[0338h] bit 6.
When this bit = 1b, the available status of LUTx is included in REG[0338h] bit 6.

A.3.17 Display Engine: Control/Trigger Registers

REG[0330h] Update Buffer Configuration Register
Default = 0000h — Read/Write

15	14	13	12	11	10	9	8
Display Engine Software Reset (WO)	n/a			Last Waveform Mode Used bits 3-0 (RO)			
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
LUT Auto Select Enable	Auto Waveform Mode Select Enable	n/a			LUT Index Format Select bits 2-0		

bit 15 Display Engine Software Reset (Write Only)
This bit performs a software reset of the display engine and resets the value of REG[0340h] ~ REG[0346h], REG[0350h], and REG[0352h] to their default values.
Writing a 0b to this bit has no effect.
Writing a 1b to this bit initiates a software reset of the display engine.

bits 11-8 Last Waveform Mode Used bits [3:0] (Read Only)
These bits indicate the waveform mode used for the last display update operation.

bit 7 LUT Auto Select Enable
This bit determines whether the Look-Up Tables (LUTs) are manually selected using the Display Update LUT Select bit (REG[0334h] bits 7-4) or automatically selected from an available LUT. If Auto LUT Select is enabled, the Display Update LUT Select bits are ignored.
When this bit = 0b, LUT auto select is disabled.
When this bit = 1b, LUT auto select is enabled.

bit 6 Auto Waveform Mode Select Enable
This bit determines whether the S1D13521 automatically selects the appropriate waveform mode. For further details, see A.3.22, “Auto Waveform Mode Configuration Registers” on page 239 and Chapter 15, “Auto Waveform Mode” on page 129.
When this bit = 0b, auto waveform mode select is disabled.
When this bit = 1b, auto waveform mode select is enabled.

bits 2-0 LUT Index Format Select bits [2:0]
These bits select the index format for the Look-Up Tables (LUTs).

Table 21-25 : LUT Index Format Selection

REG[0330h] bits 2-0	LUT Index Format
000b	P2N
001b	Reserved
010b	P3N
011b	Reserved
100b	P4N
101b	Reserved
110b	P5N
111b	Reserved

REG[0332h] Update Buffer Pixel Set Value Register
Default = 0000h Read/Write

n/a							
15	14	13	12	11	10	9	8
Update Buffer Pixel Set Value bits 7-0							
7	6	5	4	3	2	1	0

bits 7-0 Update Buffer Pixel Set Value bits [7:0]
These bits specify the pixel value used when performing an Update Buffer Set Value Refresh operation, REG[0334h] bits 3-1 = 001b. Only the most significant bits (MSb) of this value are used as determined by the LUT Index Format Select bits, REG[0330h] bits 2-0.

REG[0334h] Display Engine Control/Trigger Register
Default = 0000h Write/Read

3-Wire Chip Power Control Enable	Border Update Enable	Update Rectangle Mode bits 1-0		Display Update Waveform Mode bits 3-0			
15	14	13	12	11	10	9	8
Display Update LUT Select bits 3-0				Operation Mode bits 2-0			Operation Trigger (WO)
7	6	5	4	3	2	1	0

bit 15 3-Wire Chip Power Control Enable
This bit is only active when the Waveform data format is version 2 (voltage control format). This bit controls the 3-Wire Chip power control sequence used for programming the 3-Wire Chip (using Version 2 waveform data) on every display update trigger.
When this bit = 0b, the 3-Wire Chip power control sequence is disabled.
When this bit = 1b, the 3-Wire Chip power control sequence is enabled.

bit 14 Border Update Enable
This bit controls border updates.
When this bit = 0b, the border is not updated on the next display update (disabled).
When this bit = 1b, the border is updated on the next display update (enabled).

bits 13-12 Update Rectangle Mode bits [1:0]

These bits are used when the selected operation mode (see REG[0334h] bits 3-1) is set for Update Buffer Set Value Refresh, Update Buffer Image Buffer Refresh, Full Display Update, or Partial Display Update. These bits select the method used to define the update rectangle.

Table 21-26 : Update Rectangle Mode

REG[0334h] bits 13-12	Update Rectangle Mode
00b	Full Display Size Update
01b	Host X/Y Start/End positions are used (see REG[0348h] ~ REG[034Eh]
10b	X/Y Start/End positions are specified by REG[0340h] ~ REG[0346h]
11b	Reserved

Note

If these bits are set to use Host X/Y Start/End positions (REG[0334h] bits 13-12 = 01b), multiple Packed Pixel Rectangular transfers to the Image Buffer memory can be performed, without an Operation Write Trigger. The Host Pixel Rectangular X/Y Start/End registers are updated with the coordinates of the entire Image Buffer area encompassed by the multiple Packed Pixel Rectangular transfers. Then an Operation Write Trigger can be performed, and then only the encompassed rectangular area will be updated.

bits 11-8 Display Update Waveform Mode Select bits [3:0]

These bits are only used for Operation Modes 3 and 4 (REG[0334h] bits 3-1 = 011b and 100b). These bits select the Waveform Mode for the display update.

bits 7-4 Display Update LUT Select bits [3:0]

These bits are only used for Operation Modes 3 and 4 (REG[0334h] bits 3-1 = 011b and 100b). These bits select the LUT (from LUT0 to LUT15) that is used for the display update. If the LUT Auto Select Enable bit is set (REG[0330h] bit 7 = 1b), these bits are ignored and the LUT is automatically selected.

bits 3-1 Operation Mode Select bits [2:0]

These bits select the operation mode that is triggered when the Operation Write Trigger bit is set, REG[0334h] bit 0 = 1b.

Table 21-27 : Operation Mode Selection

REG[0334h] bits 3-1	Operation Mode
000b	Waveform Header Read
001b	Update Buffer Set Value Refresh
010b	Update Buffer Image Buffer Refresh
011b	Full Display Update
100b	Partial Display Update
101b	Gate Driver Clear Operation
110b ~ 111b	Reserved

bit 0 Operation Write Trigger (Write Only)

This bit triggers a new operation as selected by REG[0334h] bits 3-1. If a new operation is triggered while the Operation Trigger Busy bit is set (REG[0338h] bit 0 = 1b), the operation trigger is ignored and an Operation Trigger Error Interrupt occurs (see REG[033Ah] ~ REG[033Ch] bit 8).

Writing a 0b to this bit has no effect.

Writing a 1b to this bit triggers a new operation.

Note

Full updates, partial updates, and waveform header reads (REG[0334h] bits 3-1 = 011b, 100b, or 101b), should not be performed unless the SPI Flash is set for Display Engine access mode, REG[0204h] bit 7 = 1b.

A.3.18 Display Engine: Update Buffer Status Registers

REG[0336h] Lookup Table Status Register
Default = 0000h — Read Only

LUT15 Frame Update Busy	LUT14 Frame Update Busy	LUT13 Frame Update Busy	LUT12 Frame Update Busy	LUT11 Frame Update Busy	LUT10 Frame Update Busy	LUT9 Frame Update Busy	LUT8 Frame Update Busy
15	14	13	12	11	10	9	8
LUT7 Frame Update Busy	LUT6 Frame Update Busy	LUT5 Frame Update Busy	LUT4 Frame Update Busy	LUT3 Frame Update Busy	LUT2 Frame Update Busy	LUT1 Frame Update Busy	LUT0 Frame Update Busy
7	6	5	4	3	2	1	0

bits 15-0 LUT[15:0] Frame Update Busy (Read Only)
These bits indicate the status of the LUTx frame update. When a display update command for the corresponding LUT is issued, the LUT status will remain busy until all frames (N-Frames) have been transferred to the display.
When this bit = 0b, the corresponding LUT is not in use (idle).
When this bit = 1b, the corresponding LUT is in use (busy updating).

REG[0338h] Display Engine Busy Status Register
Default = 0020h — Read/Write

n/a			Serial Flash Checksum Error - N-Frame Compressed Data	Serial Flash Checksum Error - Region Pointer	Serial Flash Checksum Error - Mode Table	Serial Flash Checksum Error - Temperature Region	Serial Flash Checksum Error - Waveform Header
15	14	13	12	11	10	9	8
n/a	Masked LUT Available Status (RO)	LUT Available Status (RO)	Border Frame Busy (RO)	Display Frame Busy (RO)	Update Buffer Refresh Status (RO)	1 Frame Memory Access Busy (RO)	Operation Trigger Busy (RO)
7	6	5	4	3	2	1	0

bit 12 Serial Flash Checksum Error - N-Frame Compressed Data
This bit indicates whether a Serial Flash Checksum Error has occurred in the N-Frame Compressed Data.
When this bit = 0b, a serial flash checksum error has not occurred.
When this bit = 1b, a serial flash checksum error has occurred.

To clear this status bit, write a 1b to this bit.

bit 11 Serial Flash Checksum Error - Region Pointer
This bit indicates whether a Serial Flash Checksum Error has occurred in the Region Pointer.
When this bit = 0b, a serial flash checksum error has not occurred.
When this bit = 1b, a serial flash checksum error has occurred.

To clear this status bit, write a 1b to this bit.

bit 10 Serial Flash Checksum Error - Mode Table
This bit indicates whether a Serial Flash Checksum Error has occurred in the Mode Table.
When this bit = 0b, a serial flash checksum error has not occurred.
When this bit = 1b, a serial flash checksum error has occurred.

To clear this status bit, write a 1b to this bit.

bit 9	Serial Flash Checksum Error - Temperature Region This bit indicates whether a Serial Flash Checksum Error has occurred in the Temperature Region. When this bit = 0b, a serial flash checksum error has not occurred. When this bit = 1b, a serial flash checksum error has occurred. To clear this status bit, write a 1b to this bit.
bit 8	Serial Flash Checksum Error - Waveform Header This bit indicates whether a Serial Flash Checksum Error has occurred in the Waveform Header. When this bit = 0b, a serial flash checksum error has not occurred. When this bit = 1b, a serial flash checksum error has occurred. To clear this status bit, write a 1b to this bit.
bit 6	Masked LUT Available Status (Read Only) This bit indicates whether any of the LUTs (0-15) selected by the LUT Mask bits (REG[032Eh] bits 15-0) are currently available. When this bit = 0b, none of the selected LUTs are available. When this bit = 1b, at least one of the selected LUTs is available.
bit 5	LUT Available Status (Read Only) This bit indicates whether any LUTs are currently available. The number of available LUTs depends on the LUT Index Format, REG[0330h] bits 2-0. For P5N format, only the first 4 LUTs are available. For all other formats, all 16 LUTs are available. When this bit = 0b, no LUTs are available. When this bit = 1b, at least one LUT is available.
bit 4	Border Frame Busy (Read Only) This bit indicates whether border frames are being output. When this bit = 0b, border frames are not being output (idle). When this bit = 1b, border frames are being output (busy).
bit 3	Display Frame Busy (Read Only) This bit indicates whether display frames are being output. When this bit = 0b, display frames are not being output (idle). When this bit = 1b, display frames are being output (busy).
bit 2	Update Buffer Refresh Status (Read Only) This bit indicates the status of update buffer refresh operations where the update buffer is written with new values. When this bit = 0b, the update buffer is not being refreshed. When this bit = 1b, the update buffer is being refreshed.
bit 1	1 Frame Memory Access Busy (Read Only) This bit indicates whether the memory is being accessed and will be set during any update buffer related memory access, including memory reads for display output. When this bit = 0b, memory is not being accessed (idle). When this bit = 1b, memory is being accessed (busy).

bit 0 Operation Trigger Busy (Read Only)

This bit indicates the status of the current operation (see (REG[0334h] bits 3-1) which is triggered by the Operation Write Trigger, REG[0334h] bit 0. While the selected operation is completed, this bit is automatically reset to 0b. If a new operation is triggered while this bit is set to 1b, the operation trigger is ignored and an Operation Trigger Error Interrupt occurs (see REG[033Ah] ~ REG[033Ch] bit 8).

When this bit = 0b, an operation is not being processed (idle).

When this bit = 1b, an operation is being processed (busy).

A.3.19 Display Engine: Interrupt Registers

REG[033Ah] Display Engine Interrupt Raw Status Register Default = 0000h							Read/Write
n/a	Reserved	Image Buffer Update Incomplete Interrupt Raw Status	Serial Flash Memory Checksum Error Interrupt Raw Status	Entry Count Mismatch Interrupt Raw Status	Temperature Out of Range Interrupt Raw Status	LUT Request Error Interrupt Raw Status	Operation Trigger Error Interrupt Raw Status
15	14	13	12	11	10	9	8
LUT Area Overlap Conflict Interrupt Raw Status	Display Pipe FIFO Underflow Interrupt Raw Status	All Frames Complete Interrupt Raw Status	Update Buffer Changed Interrupt Raw Status	One LUT N-Frame Display Complete Interrupt Raw Status	Display Output 1 Frame Complete Interrupt Raw Status	Update Buffer Refresh Done Interrupt Raw Status	Operation Trigger Done Interrupt Raw Status
7	6	5	4	3	2	1	0

bit 14 Reserved
The default value for this bit is 0b.

bit 13 Image Buffer Update Incomplete Interrupt Raw Status
This bit indicates the raw status of the Image Buffer Update Incomplete Interrupt and is not masked by the Image Buffer Update Incomplete Interrupt Enable bit, REG[033Eh] bit 13. This interrupt occurs when the Display Engine begins reading data from the image buffer before the Host has completely written updated image data to the same buffer.
When this bit = 0b, a Image Buffer Update Incomplete Interrupt has not occurred.
When this bit = 1b, a Image Buffer Update Incomplete Interrupt has occurred.

To clear this status bit, write a 1b to either this bit or REG[033Ch] bit 13.

bit 12 Serial Flash Memory Checksum Error Interrupt Raw Status
This bit indicates the raw status of the Serial Flash Memory Checksum Error Interrupt and is not masked by the Serial Flash Memory Checksum Error Interrupt Enable bit, REG[033Eh] bit 12. To determine the cause of this interrupt, refer to the Serial Flash Memory Checksum Error Status bits, REG[0338h] bits 12-8.
When this bit = 0b, a Serial Flash Memory Checksum Error Interrupt has not occurred.
When this bit = 1b, a Serial Flash Memory Checksum Error Interrupt has occurred.

To clear this status bit, write a 1b to either this bit or REG[033Ch] bit 12.

bit 11 Entry Count Mismatch Interrupt Raw Status
This bit indicates the raw status of the Entry Count Mismatch Interrupt and is not masked by the Entry Count Mismatch Interrupt Enable bit, REG[033Eh] bit 11. This interrupt occurs when an unsupported entry count (see REG[0354h] bits 11-10) is selected for a Look-Up Table Index Format (see REG[0330h] bits 2-0). An entry count of 256 is only supported for index formats P2N, P3N, and P4N. An entry count of 1024 is only supported for index format P5N. If a mismatch happens this bit is set and the update operation does not start.
When this bit = 0b, an Entry Count Mismatch Interrupt has not occurred.
When this bit = 1b, an Entry Count Mismatch Interrupt has occurred.

To clear this status bit, write a 1b to either this bit or REG[033Ch] bit 11.

bit 10	Temperature Out of Range Interrupt Raw Status This bit indicates the raw status of the Temperature Out of Range Interrupt and is not masked by the Temperature Out of Range Interrupt Enable bit, REG[033Eh] bit 10. This interrupt occurs during a display frame request when the temperature is greater than, or less than, the temperature regions from the Waveform Table. When this bit = 0b, a Temperature Out of Range Interrupt has not occurred. When this bit = 1b, a Temperature Out of Range Interrupt has occurred. To clear this status bit, write a 1b to either this bit or REG[033Ch] bit 10.
bit 9	LUT Request Error Interrupt Raw Status This bit indicates the raw status of the LUT Request Error Interrupt and is not masked by the LUT Request Error Interrupt Enable bit, REG[033Eh] bit 9. This interrupt occurs an invalid LUT is requested by a triggered operation. An invalid LUT request happens when the requested LUT is currently in use (busy) or when auto LUT selection is enabled (REG[0330h] bit 7 = 1b) and no free LUTs are available. Note that for P5N index formats (see REG[0330h] bits 2-0), only the first four LUTs (0, 1, 2, and 3) are available. When this bit = 0b, a LUT Request Error Interrupt has not occurred. When this bit = 1b, a LUT Request Error Interrupt has occurred. To clear this status bit, write a 1b to either this bit or REG[033Ch] bit 9.
bit 8	Operation Trigger Error Interrupt Raw Status This bit indicates the raw status of the Operation Trigger Error Interrupt and is not masked by the Operation Trigger Error Interrupt Enable bit, REG[033Eh] bit 8. This interrupt occurs when a new operation is triggered (REG[0334h] bit 0 = 1b) while another operation is already being processed. If this happens, this bit is set and the operation trigger is ignored. When this bit = 0b, an Operation Trigger Error Interrupt has not occurred. When this bit = 1b, an Operation Trigger Error Interrupt has occurred. To clear this status bit, write a 1b to either this bit or REG[033Ch] bit 8.
bit 7	LUT Area Overlap Conflict Interrupt Raw Status This bit indicates the raw status of the LUT Area Overlap Conflict Interrupt and is not masked by the LUT Area Overlap Conflict Interrupt Enable bit, REG[033Eh] bit 7. This interrupt occurs during image buffer updates when a pixel update is required and the same pixel is currently being used for frame display (using another LUT). When this bit = 0b, a LUT Area Overlap Conflict Interrupt has not occurred. When this bit = 1b, a LUT Area Overlap Conflict Interrupt has occurred. To clear this status bit, write a 1b to either this bit or REG[033Ch] bit 7.

bit 6 Display Pipe FIFO Underflow Interrupt Raw Status
This interrupt is for debugging purposes only.
This bit indicates the raw status of the Display Pipe FIFO Underflow Interrupt and is not masked by the Display Pipe FIFO Underflow Interrupt Enable bit, REG[033Eh] bit 6.
This interrupt occurs when a new operation is triggered (REG[0334h] bit 0 = 1b) and a display pipe underflow error occurs.
When this bit = 0b, a Display Pipe FIFO Underflow Interrupt has not occurred.
When this bit = 1b, a Display Pipe FIFO Underflow Interrupt has occurred.

To clear this status bit, write a 1b to either this bit or REG[033Ch] bit 6.

bit 5 All Frames Completed Interrupt Raw Status
This bit indicates the raw status of the All Frames Completed Interrupt and is not masked by the All Frames Completed Interrupt Enable bit, REG[033Eh] bit 5. This interrupt occurs at the end of a display output operation when all frames are completed.
When this bit = 0b, an All Frames Completed Interrupt has not occurred.
When this bit = 1b, an All Frames Completed Interrupt has occurred.

To clear this status bit, write a 1b to either this bit or REG[033Ch] bit 5.

bit 4 Update Buffer Changed Interrupt Raw Status
This bit indicates the raw status of the Update Buffer Changed Interrupt and is not masked by the Update Buffer Changed Interrupt Enable bit, REG[033Eh] bit 4. This interrupt occurs on every write to the update buffer and may trigger multiple times even when the update buffer has not been completely updated.
When this bit = 0b, an Update Buffer Changed Interrupt has not occurred.
When this bit = 1b, an Update Buffer Changed Interrupt has occurred.

To clear this status bit, write a 1b to either this bit or REG[033Ch] bit 4.

bit 3 One LUT N-Frame Display Complete Interrupt Raw Status
This bit indicates the raw status of the One LUT N-Frame Display Complete Interrupt and is not masked by the One LUT N-Frame Display Complete Interrupt Enable bit, REG[033Eh] bit 3. This interrupt occurs when the N-Frames required for a LUT to update a pixel or pixels completes.
When this bit = 0b, a One LUT N-Frame Display Complete Interrupt has not occurred.
When this bit = 1b, a One LUT N-Frame Display Complete Interrupt has occurred.

To clear this status bit, write a 1b to either this bit or REG[033Ch] bit 3.

bit 2 Display Output 1 Frame Complete Interrupt Raw Status
This bit indicates the raw status of the Display Output 1 Frame Complete Interrupt and is not masked by the Display Output 1 Frame Complete Interrupt Enable bit, REG[033Eh] bit 2. This interrupt occurs when display output of 1 Frame to the output Gate and Source drivers completes.
When this bit = 0b, a Display Output 1 Frame Complete Interrupt has not occurred.
When this bit = 1b, a Display Output 1 Frame Complete Interrupt has occurred.

To clear this status bit, write a 1b to either this bit or REG[033Ch] bit 2.

bit 1 Update Buffer Refresh Done Interrupt Raw Status
This bit indicates the raw status of the Update Buffer Refresh Done Interrupt and is not masked by the Update Buffer Refresh Done Interrupt Enable bit, REG[033Eh] bit 1. This interrupt occurs when an update buffer refresh operation (Set Value, Refresh, Partial Update, or Full Update; see REG[0334h] bits 3-1) completes.
When this bit = 0b, an Update Buffer Refresh Done Interrupt has not occurred.
When this bit = 1b, an Update Buffer Refresh Done Interrupt has occurred.

To clear this status bit, write a 1b to either this bit or REG[033Ch] bit 1.

bit 0 Operation Trigger Done Interrupt Raw Status
This bit indicates the raw status of the Operation Trigger Done Interrupt and is not masked by the Operation Trigger Done Interrupt Enable bit, REG[033Eh] bit 0. This interrupt occurs when the operation triggered by REG[0334h] bit 0 is completes.
When this bit = 0b, an Operation Trigger Done Interrupt has not occurred.
When this bit = 1b, an Operation Trigger Done Interrupt has occurred.

To clear this status bit, write a 1b to either this bit or REG[033Ch] bit 0.

REG[033Ch] Display Engine Interrupt Masked Status Register
Default = 0000h Read/Write

n/a	Reserved	Image Buffer Update Incomplete Interrupt Masked Status	Serial Flash Memory Checksum Error Interrupt Masked Status	Entry Count Mismatch Interrupt Masked Status	Temperature Out of Range Interrupt Masked Status	LUT Request Error Interrupt Masked Status	Operation Trigger Error Interrupt Masked Status
15	14	13	12	11	10	9	8
LUT Area Overlap Conflict Interrupt Masked Status	Display Pipe FIFO Underflow Interrupt Masked Status	All Frames Complete Interrupt Masked Status	Update Buffer Changed Interrupt Masked Status	One LUT N-Frame Display Complete Interrupt Masked Status	Display Output 1 Frame Complete Interrupt Masked Status	Update Buffer Refresh Done Interrupt Masked Status	Operation Trigger Done Interrupt Masked Status
7	6	5	4	3	2	1	0

bit 14 Reserved
The default value for this bit is 0b.

bit 13 Image Buffer Update Incomplete Interrupt Masked Status
This bit indicates the masked status of the Image Buffer Update Incomplete Interrupt (see REG[033Eh] bit 13). This interrupt occurs when the Display Engine begins reading data from the image buffer before the Host has completely written updated image data to the same buffer.
When this bit = 0b, a Image Buffer Update Incomplete Interrupt has not occurred.
When this bit = 1b, a Image Buffer Update Incomplete Interrupt has occurred.

To clear this status bit, write a 1b to either this bit or REG[033Ah] bit 13.

bit 12 Serial Flash Memory Checksum Error Interrupt Masked Status
This bit indicates the masked status of the Serial Flash Memory Checksum Error Interrupt (see REG[033Eh] bit 12). To determine the cause of this interrupt, refer to the Serial Flash Memory Checksum Error Status bits, REG[0338h] bits 12-8.
When this bit = 0b, a Serial Flash Memory Checksum Error Interrupt has not occurred.
When this bit = 1b, a Serial Flash Memory Checksum Error Interrupt has occurred.

To clear this status bit, write a 1b to either this bit or REG[033Ah] bit 12.

bit 11 Entry Count Mismatch Interrupt Masked Status
This bit indicates the masked status of the Entry Count Mismatch Interrupt (see REG[033Eh] bit 11). This interrupt occurs when an unsupported entry count (see REG[0354h] bits 11-10) is selected for a Look-Up Table Index Format (see REG[0330h] bits 2-0). An entry count of 256 is only supported for index formats P2N, P3N, and P4N. An entry count of 1024 is only supported for index format P5N. If a mismatch happens this bit is set and the update operation does not start.
When this bit = 0b, an Entry Count Mismatch Interrupt has not occurred.
When this bit = 1b, an Entry Count Mismatch Interrupt has occurred.

To clear this status bit, write a 1b to either this bit or REG[033Ah] bit 11.

bit 10 Temperature Out of Range Interrupt Masked Status
This bit indicates the masked status of the Temperature Out of Range Interrupt (see REG[033Eh] bit 10). This interrupt occurs during a display frame request when the temperature is greater than, or less than, the temperature regions from the Waveform Table.
When this bit = 0b, a Temperature Out of Range Interrupt has not occurred.
When this bit = 1b, a Temperature Out of Range Interrupt has occurred.

To clear this status bit, write a 1b to either this bit or REG[033Ah] bit 10.

bit 9 LUT Request Error Interrupt Masked Status
This bit indicates the masked status of the LUT Request Error Interrupt (see REG[033Eh] bit 9). This interrupt occurs an invalid LUT is requested by a triggered operation. An invalid LUT request happens when the requested LUT is currently in use (busy) or when auto LUT selection is enabled (REG[0330h] bit 7 = 1b) and no free LUTs are available. Note that for P5N index formats (see REG[0330h] bits 2-0), only the first four LUTs (0, 1, 2, and 3) are available.
When this bit = 0b, a LUT Request Error Interrupt has not occurred.
When this bit = 1b, a LUT Request Error Interrupt has occurred.

To clear this status bit, write a 1b to either this bit or REG[033Ah] bit 9.

bit 8 Operation Trigger Error Interrupt Masked Status
This bit indicates the masked status of the Operation Trigger Error Interrupt (see REG[033Eh] bit 8). This interrupt occurs when a new operation is triggered (REG[0334h] bit 0 = 1b) while another operation is already being processed. If this happens, this bit is set and the operation trigger is ignored.
When this bit = 0b, an Operation Trigger Error Interrupt has not occurred.
When this bit = 1b, an Operation Trigger Error Interrupt has occurred.

To clear this status bit, write a 1b to either this bit or REG[033Ah] bit 8.

bit 7 LUT Area Overlap Conflict Interrupt Masked Status
This bit indicates the masked status of the LUT Area Overlap Conflict Interrupt (see REG[033Eh] bit 7). This interrupt occurs during image buffer updates when a pixel update is required and the same pixel is currently being used for frame display (using another LUT).
When this bit = 0b, a LUT Area Overlap Conflict Interrupt has not occurred.
When this bit = 1b, a LUT Area Overlap Conflict Interrupt has occurred.

To clear this status bit, write a 1b to either this bit or REG[033Ah] bit 7.

bit 6 Display Pipe FIFO Underflow Interrupt Masked Status
This interrupt is for debugging purposes only.
This bit indicates the masked status of the Display Pipe FIFO Underflow Interrupt (see REG[033Eh] bit 6). This interrupt occurs when a new operation is triggered (REG[0334h] bit 0 = 1b) and a display pipe underflow error occurs.
When this bit = 0b, a Display Pipe FIFO Underflow Interrupt has not occurred.
When this bit = 1b, a Display Pipe FIFO Underflow Interrupt has occurred.

To clear this status bit, write a 1b to either this bit or REG[033Ah] bit 6.

bit 5 All Frames Completed Interrupt Masked Status
This bit indicates the masked status of the All Frames Completed Interrupt (see REG[033Eh] bit 5). This interrupt occurs at the end of a display output operation when all frames are completed.
When this bit = 0b, an All Frames Completed Interrupt has not occurred.
When this bit = 1b, an All Frames Completed Interrupt has occurred.

To clear this status bit, write a 1b to either this bit or REG[033Ah] bit 5.

bit 4 Update Buffer Changed Interrupt Masked Status
This bit indicates the masked status of the Update Buffer Changed Interrupt (see REG[033Eh] bit 4). This interrupt occurs on every write to the update buffer and may trigger multiple times even when the update buffer has not been completely updated.
When this bit = 0b, an Update Buffer Changed Interrupt has not occurred.
When this bit = 1b, an Update Buffer Changed Interrupt has occurred.

To clear this status bit, write a 1b to either this bit or REG[033Ah] bit 4.

bit 3 One LUT N-Frame Display Complete Interrupt Masked Status
This bit indicates the masked status of the One LUT N-Frame Display Complete Interrupt (see REG[033Eh] bit 3). This interrupt occurs when the N-Frames required for a LUT to update a pixel or pixels completes.
When this bit = 0b, a One LUT N-Frame Display Complete Interrupt has not occurred.
When this bit = 1b, a One LUT N-Frame Display Complete Interrupt has occurred.

To clear this status bit, write a 1b to either this bit or REG[033Ah] bit 3.

bit 2 Display Output 1 Frame Complete Interrupt Masked Status
This bit indicates the masked status of the Display Output 1 Frame Complete Interrupt (see REG[033Eh] bit 2). This interrupt occurs when display output of 1 Frame to the output Gate and Source drivers completes.
When this bit = 0b, a Display Output 1 Frame Complete Interrupt has not occurred.
When this bit = 1b, a Display Output 1 Frame Complete Interrupt has occurred.

To clear this status bit, write a 1b to either this bit or REG[033Ah] bit 2.

bit 1 Update Buffer Refresh Done Interrupt Masked Status
This bit indicates the masked status of the Update Buffer Refresh Done Interrupt (see REG[033Eh] bit 1). This interrupt occurs when an update buffer refresh operation (Set Value, Refresh, Partial Update, or Full Update; see REG[0334h] bits 3-1) completes.
When this bit = 0b, an Update Buffer Refresh Done Interrupt has not occurred.
When this bit = 1b, an Update Buffer Refresh Done Interrupt has occurred.

To clear this status bit, write a 1b to either this bit or REG[033Ah] bit 1.

bit 0 Operation Trigger Done Interrupt Masked Status
This bit indicates the masked status of the Operation Trigger Done Interrupt (see REG[033Eh] bit 0). This interrupt occurs when the operation triggered by REG[0334h] bit 0 is completes.
When this bit = 0b, an Operation Trigger Done Interrupt has not occurred.
When this bit = 1b, an Operation Trigger Done Interrupt has occurred.

To clear this status bit, write a 1b to either this bit or REG[033Ah] bit 0.

REG[033Eh] Display Engine Interrupt Enable Register
Default = 0000h Read/Write

n/a	Reserved	Image Buffer Update Incomplete Interrupt Enable	Serial Flash Memory Checksum Error Interrupt Enable	Entry Count Mismatch Interrupt Enable	Temperature Out of Range Interrupt Enable	LUT Request Error Interrupt Enable	Operation Trigger Error Interrupt Enable
15	14	13	12	11	10	9	8
LUT Area Overlap Conflict Interrupt Enable	Display Pipe FIFO Underflow Interrupt Enable	All Frames Complete Interrupt Enable	Update Buffer Changed Interrupt Enable	One LUT N-Frame Display Complete Interrupt Enable	Display Output 1 Frame Complete Interrupt Enable	Update Buffer Refresh Done Interrupt Enable	Operation Trigger Done Interrupt Enable
7	6	5	4	3	2	1	0

bit 14 Reserved
The default value for this bit is 0b.

bit 13 Image Buffer Update Incomplete Interrupt Enable
This bit controls whether the Image Buffer Update Incomplete Interrupt triggers a Display Engine Interrupt (see REG[0240h] and REG[0242h]). The status of this interrupt can be determined by reading REG[033Ah] bit 13 (unmasked) or REG[033Ch] bit 13 (masked).
When this bit = 0b, the interrupt is disabled.
When this bit = 1b, the interrupt is enabled.

bit 12	Serial Flash Memory Checksum Error Interrupt Enable This bit controls whether the Serial Flash Memory Checksum Error Interrupt triggers a Display Engine Interrupt (see REG[0240h] and REG[0242h]). The status of this interrupt can be determined by reading REG[033Ah] bit 12 (unmasked) or REG[033Ch] bit 12 (masked). When this bit = 0b, the interrupt is disabled. When this bit = 1b, the interrupt is enabled.
bit 11	Entry Count Mismatch Interrupt Enable This bit controls whether the Entry Count Mismatch Interrupt triggers a Display Engine Interrupt (see REG[0240h] and REG[0242h]). The status of this interrupt can be determined by reading REG[033Ah] bit 11 (unmasked) or REG[033Ch] bit 11 (masked). When this bit = 0b, the interrupt is disabled. When this bit = 1b, the interrupt is enabled.
bit 10	Temperature Out of Range Interrupt Enable This bit controls whether the Temperature Out of Range Interrupt triggers a Display Engine Interrupt (see REG[0240h] and REG[0242h]). The status of this interrupt can be determined by reading REG[033Ah] bit 10 (unmasked) or REG[033Ch] bit 10 (masked). When this bit = 0b, the interrupt is disabled. When this bit = 1b, the interrupt is enabled.
bit 9	LUT Request Error Interrupt Enable This bit controls whether the LUT Request Error Interrupt triggers a Display Engine Interrupt (see REG[0240h] and REG[0242h]). The status of this interrupt can be determined by reading REG[033Ah] bit 9 (unmasked) or REG[033Ch] bit 9 (masked). When this bit = 0b, the interrupt is disabled. When this bit = 1b, the interrupt is enabled.
bit 8	Operation Trigger Error Interrupt Enable This bit controls whether the Operation Trigger Error Interrupt triggers a Display Engine Interrupt (see REG[0240h] and REG[0242h]). The status of this interrupt can be determined by reading REG[033Ah] bit 8 (unmasked) or REG[033Ch] bit 8 (masked). When this bit = 0b, the interrupt is disabled. When this bit = 1b, the interrupt is enabled.
bit 7	LUT Area Overlap Conflict Interrupt Enable This bit controls whether the LUT Area Overlap Conflict Interrupt triggers a Display Engine Interrupt (see REG[0240h] and REG[0242h]). The status of this interrupt can be determined by reading REG[033Ah] bit 7 (unmasked) or REG[033Ch] bit 7 (masked). When this bit = 0b, the interrupt is disabled. When this bit = 1b, the interrupt is enabled.
bit 6	Display Pipe FIFO Underflow Interrupt Enable This interrupt is for debugging purposes only. This bit controls whether the Display Pipe FIFO Underflow Interrupt triggers a Display Engine Interrupt (see REG[0240h] and REG[0242h]). The status of this interrupt can be determined by reading REG[033Ah] bit 6 (unmasked) or REG[033Ch] bit 6 (masked). When this bit = 0b, the interrupt is disabled. When this bit = 1b, the interrupt is enabled.

bit 5 — All Frames Complete Interrupt Enable
This bit controls whether the All Frames Complete Interrupt triggers a Display Engine Interrupt (see REG[0240h] and REG[0242h]). The status of this interrupt can be determined by reading REG[033Ah] bit 5 (unmasked) or REG[033Ch] bit 5 (masked).
When this bit = 0b, the interrupt is disabled.
When this bit = 1b, the interrupt is enabled.

bit 4 — Update Buffer Changed Interrupt Enable
This bit controls whether the Update Buffer Changed Interrupt triggers a Display Engine Interrupt (see REG[0240h] and REG[0242h]). The status of this interrupt can be determined by reading REG[033Ah] bit 4 (unmasked) or REG[033Ch] bit 4 (masked).
When this bit = 0b, the interrupt is disabled.
When this bit = 1b, the interrupt is enabled.

bit 3 — One LUT N-Frame Display Complete Interrupt Enable
This bit controls whether the One LUT N-Frame Display Complete Interrupt triggers a Display Engine Interrupt (see REG[0240h] and REG[0242h]). The status of this interrupt can be determined by reading REG[033Ah] bit 3 (unmasked) or REG[033Ch] bit 3 (masked).
When this bit = 0b, the interrupt is disabled.
When this bit = 1b, the interrupt is enabled.

bit 2 — Display Output 1 Frame Complete Interrupt Enable
This bit controls whether the Display Output 1 Frame Complete Interrupt triggers a Display Engine Interrupt (see REG[0240h] and REG[0242h]). The status of this interrupt can be determined by reading REG[033Ah] bit 2 (unmasked) or REG[033Ch] bit 2 (masked).
When this bit = 0b, the interrupt is disabled.
When this bit = 1b, the interrupt is enabled.

bit 1 — Update Buffer Refresh Done Interrupt Enable
This bit controls whether the Update Buffer Refresh Done Interrupt triggers a Display Engine Interrupt (see REG[0240h] and REG[0242h]). The status of this interrupt can be determined by reading REG[033Ah] bit 1 (unmasked) or REG[033Ch] bit 1 (masked).
When this bit = 0b, the interrupt is disabled.
When this bit = 1b, the interrupt is enabled.

bit 0 — Operation Trigger Done Interrupt Enable
This bit controls whether the Operation Trigger Done Interrupt triggers a Display Engine Interrupt (see REG[0240h] and REG[0242h]). The status of this interrupt can be determined by reading REG[033Ah] bit 0 (unmasked) or REG[033Ch] bit 0 (masked).
When this bit = 0b, the interrupt is disabled.
When this bit = 1b, the interrupt is enabled.

A.3.20 Display Engine: Partial Update Configuration Register

REG[0340h] Area Update Pixel Rectangular X-Start Register
Default = 0000h — Read/Write

n/a			Reserved	Area Update Pixel Rectangular X-Start Position bits 11-8			
15	14	13	12	11	10	9	8
Area Update Pixel Rectangular X-Start Position bits 7-0							
7	6	5	4	3	2	1	0

bit 12 Reserved
The default value for this bit is 0b.

bits 11-0 Area Update Pixel Rectangular X-Start Position bits [11:0]
When the Update Rectangle Mode bits are set for user configured X/Y Start/End (REG[0334h] bits 13-12 = 10b), these bits specify the X start position of the rectangular area to be updated, relative to the top left of the rotated image.

Note

1. The X-Start, Y-Start coordinates must be set within the display area.
2. These bits are updated by the Display Engine with the coordinates of the area encompassed by the update after each Operation Write Trigger - depending on the Update Rectangle Mode. For Full Display Size Update mode (REG[0334h] bits 13-12 = 00b), the Operation Write Trigger will cause REG[0340h] ~ REG[0346h] to be updated with the coordinates of the display size. When Host X/Y Start/End positions are used (REG[0334h] bits 13-12 = 01b), the Operation Write Trigger will cause REG[0340h] ~ REG[0346h] to be updated with the coordinates from REG[0348h] ~ REG[034Eh]. When the X/Y Start/End positions are used (REG[0334h] bits 13-12 = 10b), the Operation Write Trigger will cause REG[0340h] ~ REG[0346h] to be updated with the coordinates from REG[0340h] ~ REG[0346h].

REG[0342h] Area Update Pixel Rectangular Y-Start Register

Default = 0000h — Read/Write

n/a			Reserved	Area Update Pixel Rectangular Y-Start Position bits 11-8			
15	14	13	12	11	10	9	8
Area Update Pixel Rectangular Y-Start Position bits 7-0							
7	6	5	4	3	2	1	0

bit 12 Reserved
The default value for this bit is 0b.

bits 11-0 Area Update Pixel Rectangular Y-Start Position bits [11:0]
When the Update Rectangle Mode bits are set for user configured X/Y Start/End (REG[0334h] bits 13-12 = 10b), these bits specify the Y start position of the rectangular area to be updated, relative to the top left of the rotated image.

Note

1. The X-Start, Y-Start coordinates must be set within the display area.
2. These bits are updated by the Display Engine with the coordinates of the area encompassed by the update after each Operation Write Trigger - depending on the Update Rectangle Mode. For Full Display Size Update mode (REG[0334h] bits 13-12 = 00b), the Operation Write Trigger will cause REG[0340h] ~ REG[0346h] to be updated with the coordinates of the display size. When Host X/Y Start/End positions are used (REG[0334h] bits 13-12 = 01b), the Operation Write Trigger will cause REG[0340h] ~ REG[0346h] to be updated with the coordinates from REG[0348h] ~ REG[034Eh]. When the X/Y Start/End positions are used (REG[0334h] bits 13-12 = 10b), the Operation Write Trigger will cause REG[0340h] ~ REG[0346h] to be updated with the coordinates from REG[0340h] ~ REG[0346h].

REG[0344h] Area Update Pixel Rectangular X-End / Horizontal Size Register

Default = 0000h Read/Write

n/a			Area Update Pixel Rectangular X-End Position / Horizontal Size bits 12-8				
15	14	13	12	11	10	9	8
Area Update Pixel Rectangular X-End Position / Horizontal Size bits 7-0							
7	6	5	4	3	2	1	0

bits 12-0 Area Update Pixel Rectangular X-End Position / Horizontal Size bits [12:0]
When the Update Rectangle Mode bits are set for user configured X/Y Start/End (REG[0334h] bits 13-12 = 10b), these bits specify either the X end position or the horizontal size (see REG[032Ch] bit 10) of the rectangular area to be updated, relative to the top left of the rotated image.

Note

1. The X-End, Y-End coordinates must be set within the display area.
2. These bits are updated by the Display Engine with the coordinates of the area encompassed by the update after each Operation Write Trigger - depending on the Update Rectangle Mode. For Full Display Size Update mode (REG[0334h] bits 13-12 = 00b), the Operation Write Trigger will cause REG[0340h] ~ REG[0346h] to be updated with the coordinates of the display size. When Host X/Y Start/End positions are used (REG[0334h] bits 13-12 = 01b), the Operation Write Trigger will cause REG[0340h] ~ REG[0346h] to be updated with the coordinates from REG[0348h] ~ REG[034Eh]. When the X/Y Start/End positions are used (REG[0334h] bits 13-12 = 10b), the Operation Write Trigger will cause REG[0340h] ~ REG[0346h] to be updated with the coordinates from REG[0340h] ~ REG[0346h].

REG[0346h] Area Update Pixel Rectangular Y-End / Vertical Size Register

Default = 0000h Read/Write

n/a			Area Update Pixel Rectangular Y-End Position / Vertical Size bits 12-8				
15	14	13	12	11	10	9	8
Area Update Pixel Rectangular Y-End Position / Vertical Size bits 7-0							
7	6	5	4	3	2	1	0

bits 12-0 Area Update Pixel Rectangular Y-End Position / Vertical Size bits [12:0]
When the Update Rectangle Mode bits are set for user configured X/Y Start/End (REG[0334h] bits 13-12 = 10b), these bits specify either the Y end position or the vertical size (see REG[032Ch] bit 10) of the rectangular area to be updated, relative to the top left of the rotated image.

Note

1. The X-End, Y-End coordinates must be set within the display area.
2. These bits are updated by the Display Engine with the coordinates of the area encompassed by the update after each Operation Write Trigger - depending on the Update Rectangle Mode. For Full Display Size Update mode (REG[0334h] bits 13-12 = 00b), the Operation Write Trigger will cause REG[0340h] ~ REG[0346h] to be updated with the coordinates of the display size. When Host X/Y Start/End positions are used (REG[0334h] bits 13-12 = 01b), the Operation Write Trigger will cause REG[0340h] ~ REG[0346h] to be updated with the coordinates from REG[0348h] ~ REG[034Eh]. When the X/Y Start/End positions are used (REG[0334h] bits 13-12 = 10b), the Operation Write Trigger will cause REG[0340h] ~ REG[0346h] to be updated with the coordinates from REG[0340h] ~ REG[0346h].

REG[0348h] Host Pixel Rectangular X-Start Register
Default = 1FFFh — Read Only

n/a			Host Pixel Rectangular X-Start Position bits 12-8				
15	14	13	12	11	10	9	8
Host Pixel Rectangular X-Start Position bits 7-0							
7	6	5	4	3	2	1	0

bits 12-0 Host Pixel Rectangular X-Start Position bits [12:0] (Read Only)
When the Update Rectangle Mode bits are set to use Host X/Y Start/End (REG[0334h] bits 13-12 = 01b), these bits indicate the X start position of the rectangular area that is updated. These bits should only be read after the packed pixel rectangular transfers to the image buffer are complete. If multiple packed pixel rectangular transfers are performed without an operation write trigger, the Host Pixel Rectangular X/Y Start End positions will be expanded to encompass the entire area affected by the multiple writes.

Note
The X-Start, Y-Start coordinates must be set within the display area.

REG[034Ah] Host Pixel Rectangular Y-Start Register
Default = 1FFFh — Read Only

n/a			Host Pixel Rectangular Y-Start Position bits 12-8				
15	14	13	12	11	10	9	8
Host Pixel Rectangular Y-Start Position bits 7-0							
7	6	5	4	3	2	1	0

bits 12-0 Host Pixel Rectangular Y-Start Position bits [12:0] (Read Only)
When the Update Rectangle Mode bits are set to use Host X/Y Start/End (REG[0334h] bits 13-12 = 01b), these bits indicate the Y start position of the rectangular area that is updated. These bits should only be read after the packed pixel rectangular transfers to the image buffer are complete. If multiple packed pixel rectangular transfers are performed without an operation write trigger, the Host Pixel Rectangular X/Y Start End positions will be expanded to encompass the entire area affected by the multiple writes.

Note
The X-Start, Y-Start coordinates must be set within the display area.

REG[034Ch] Host Pixel Rectangular X-End Register
Default = 0000h — Read Only

n/a			Host Pixel Rectangular X-End Position bits 12-8				
15	14	13	12	11	10	9	8
Host Pixel Rectangular X-End Position bits 7-0							
7	6	5	4	3	2	1	0

bits 12-0 Host Pixel Rectangular X-End Position bits [12:0] (Read Only)
When the Update Rectangle Mode bits are set to use Host X/Y Start/End (REG[0334h] bits 13-12 = 01b), these bits indicate the X end position of the rectangular area that is updated. These bits should only be read after the packed pixel rectangular transfers to the image buffer are complete. If multiple packed pixel rectangular transfers are performed without an operation write trigger, the Host Pixel Rectangular X/Y Start End positions will be expanded to encompass the entire area affected by the multiple writes.

Note
The X-End, Y-End coordinates must be set within the display area.

REG[034Eh] Host Pixel Rectangular Y-End Register
Default = 0000h — Read Only

n/a			Host Pixel Rectangular Y-End Position bits 12-8				
15	14	13	12	11	10	9	8
Host Pixel Rectangular Y-End Position bits 7-0							
7	6	5	4	3	2	1	0

bits 12-0 Host Pixel Rectangular Y-End Position bits [12:0] (Read Only)
When the Update Rectangle Mode bits are set to use Host X/Y Start/End (REG[0334h] bits 13-12 = 01b), these bits indicate the Y end position of the rectangular area that is updated. These bits should only be read after the packed pixel rectangular transfers to the image buffer are complete. If multiple packed pixel rectangular transfers are performed without an operation write trigger, the Host Pixel Rectangular X/Y Start End positions will be expanded to encompass the entire area affected by the multiple writes.

Note
The X-End, Y-End coordinates must be set within the display area.

A.3.21 Display Engine: Serial Flash Waveform Registers

REG[0350h] Waveform Header Serial Flash Address Register 0
Default = 0000h — Read/Write

15	14	13	12	11	10	9	8
Waveform Header Serial Flash Address bits 15-8							
7	6	5	4	3	2	1	0
Waveform Header Serial Flash Address bits 7-0							

REG[0352h] Waveform Header Serial Flash Address Register 1
Default = 0000h — Read/Write

15	14	13	12	11	10	9	8
n/a							
7	6	5	4	3	2	1	0
Waveform Header Serial Flash Address bits 23-16							

REG[0352h] bits 7-0
REG[0350h] bits 15-0 Waveform Header Serial Flash Address bits [23:0]
These bits store the Waveform Header start address in the Flash Memory.

REG[0354h] through REG[035Eh] are Reserved

These registers are Reserved and should not be written.

A.3.22 Auto Waveform Mode Configuration Registers

When Auto Waveform Mode is selected (REG[0330h] bit 6 = 1b), these bits are used to set the waveform mode based on the amount of change between the current pixel value and the next pixel value. Four (0-3) waveform modes can be programmed with Auto Waveform Mode Compare 0 having the highest priority and Auto Waveform Mode Compare 3 having the lowest priority. The waveform mode is selected when the pixel value change reaches the highest priority minimum threshold level. Additionally, the current and next pixel values can be compared to specified values allowing different waveform modes to be configured for pixel changes of the same value, but between different colors (i.e. from black to white or from white to black).

For example, if the pixel change is greater than or equal to the minimum threshold and the current/next pixel values are equal to the specified values (when enabled), the Auto Waveform Mode number is used. If the minimum threshold is not reached or the current/next pixel values are not equal to the specified values (when enabled), the next highest priority Auto Waveform Mode Compare minimum threshold is checked. If all compare thresholds are checked, but the pixel change and pixel value conditions are not met, a Auto Waveform Mode Select Error is generated (see REG[0240h] ~ REG[0244h] bit 9).

REG[0360h] Auto Waveform Mode Compare 0 Configuration Register
Default = 0001h — Read/Write

Compare 0 Pixel Change Minimum Threshold bits 7-0							
15	14	13	12	11	10	9	8
Compare 0 Current Pixel Value Compare Enable	Compare 0 Next Pixel Value Compare Enable	n/a		Compare 0 Waveform Mode Number bits 3-0			
7	6	5	4	3	2	1	0

REG[0362h] Auto Waveform Mode Compare 0 Current/Next Register
Default = 0000h — Read/Write

Compare 0 Current Pixel Value bits 7-0							
15	14	13	12	11	10	9	8
Compare 0 Next Pixel Value bits 7-0							
7	6	5	4	3	2	1	0

REG[0360h] bits 15-8 Compare 0 Pixel Change Minimum Threshold bits [7:0]
When Auto Waveform Mode is selected (REG[0330h] bit 6 = 1b), these bits specify the pixel change minimum threshold for Compare 0.

REG[0360h] bit 7 Compare 0 Current Pixel Value Compare Enable
When Auto Waveform Mode is selected (REG[0330h] bit 6 = 1b), this bit determines whether the current pixel value is compared for Compare 0.
When this bit = 0b, the current pixel value is not compared.
When this bit = 1b, the current pixel value is compared with the value specified by the Compare 0 Current Pixel Value bits, REG[0362h] bits 15-8.

REG[0360h] bit 6 Compare 0 Next Pixel Value Compare Enable
When Auto Waveform Mode is selected (REG[0330h] bit 6 = 1b), this bit determines whether the next pixel value is compared for Compare 0.
When this bit = 0b, the next pixel value is not compared.
When this bit = 1b, the next pixel value is compared with the value specified by the Compare 0 Next Pixel Value bits, REG[0362h] bits 7-0.

REG[0360h] bits 3-0 Compare 0 Waveform Mode Number bits [3:0]
When Auto Waveform Mode is selected (REG[0330h] bit 6 = 1b), these bits specify the waveform mode number used if the pixel change is greater than or equal to the minimum threshold and the current/next pixel values are equal to the specified values (when enabled).

REG[0362h] bits 15-8 Compare 0 Current Pixel Value bits [7:0]
When Auto Waveform Mode is selected (REG[0330h] bit 6 = 1b) and Compare 0 Current Pixel Value Compare is enabled (REG[0360h] bit 7 = 1b), these bits specify the pixel value that is compared with the current pixel value for Compare 0.

REG[0362h] bits 7-0 Compare 0 Next Pixel Value bits [7:0]
When Auto Waveform Mode is selected (REG[0330h] bit 6 = 1b) and Compare 0 Next Pixel Value Compare is enabled (REG[0360h] bit 6 = 1b), these bits specify the pixel value that is compared with the next pixel value for Compare 0.

REG[0364h] Auto Waveform Mode Compare 1 Configuration Register
Default = 0001h — Read/Write

Compare 1 Pixel Change Minimum Threshold bits 7-0							
15	14	13	12	11	10	9	8
Compare 1 Current Pixel Value Compare Enable	Compare 1 Next Pixel Value Compare Enable	n/a		Compare 1 Waveform Mode Number bits 3-0			
7	6	5	4	3	2	1	0

REG[0366h] Auto Waveform Mode Compare 1 Current/Next Register
Default = 0000h — Read/Write

Compare 1 Current Pixel Value bits 7-0							
15	14	13	12	11	10	9	8
Compare 1 Next Pixel Value bits 7-0							
7	6	5	4	3	2	1	0

REG[0364h] bits 15-8 Compare 1 Pixel Change Minimum Threshold bits [7:0]
When Auto Waveform Mode is selected (REG[0330h] bit 6 = 1b), these bits specify the pixel change minimum threshold for Compare 1.

REG[0364h] bit 7 Compare 1 Current Pixel Value Compare Enable
When Auto Waveform Mode is selected (REG[0330h] bit 6 = 1b), this bit determines whether the current pixel value is compared for Compare 1.
When this bit = 0b, the current pixel value is not compared.
When this bit = 1b, the current pixel value is compared with the value specified by the Compare 1 Current Pixel Value bits, REG[0366h] bits 15-8.

REG[0364h] bit 6 Compare 1 Next Pixel Value Compare Enable
When Auto Waveform Mode is selected (REG[0330h] bit 6 = 1b), this bit determines whether the next pixel value is compared for Compare 1.
When this bit = 0b, the next pixel value is not compared.
When this bit = 1b, the next pixel value is compared with the value specified by the Compare 1 Next Pixel Value bits, REG[0366h] bits 7-0.

REG[0364h] bits 3-0 Compare 1 Waveform Mode Number bits [3:0]
When Auto Waveform Mode is selected (REG[0330h] bit 6 = 1b), these bits specify the waveform mode number used if the pixel change is greater than or equal to the minimum threshold and the current/next pixel values are equal to the specified values (when enabled).

REG[0366h] bits 15-8 Compare 1 Current Pixel Value bits [7:0]
When Auto Waveform Mode is selected (REG[0330h] bit 6 = 1b) and Compare 1 Current Pixel Value Compare is enabled (REG[0364h] bit 7 = 1b), these bits specify the pixel value that is compared with the current pixel value for Compare 1.

REG[0366h] bits 7-0 Compare 1 Next Pixel Value bits [7:0]
When Auto Waveform Mode is selected (REG[0330h] bit 6 = 1b) and Compare 1 Next Pixel Value Compare is enabled (REG[0364h] bit 6 = 1b), these bits specify the pixel value that is compared with the next pixel value for Compare 1.

REG[0368h] Auto Waveform Mode Compare 2 Configuration Register
Default = 0001h — Read/Write

Compare 2 Pixel Change Minimum Threshold bits 7-0							
15	14	13	12	11	10	9	8
Compare 2 Current Pixel Value Compare Enable	Compare 2 Next Pixel Value Compare Enable	n/a		Compare 2 Waveform Mode Number bits 3-0			
7	6	5	4	3	2	1	0

REG[036Ah] Auto Waveform Mode Compare 2 Current/Next Register
Default = 0000h — Read/Write

Compare 2 Current Pixel Value bits 7-0							
15	14	13	12	11	10	9	8
Compare 2 Next Pixel Value bits 7-0							
7	6	5	4	3	2	1	0

REG[0368h] bits 15-8 Compare 2 Pixel Change Minimum Threshold bits [7:0]
When Auto Waveform Mode is selected (REG[0330h] bit 6 = 1b), these bits specify the pixel change minimum threshold for Compare 2.

REG[0368h] bit 7 Compare 2 Current Pixel Value Compare Enable
When Auto Waveform Mode is selected (REG[0330h] bit 6 = 1b), this bit determines whether the current pixel value is compared for Compare 2.
When this bit = 0b, the current pixel value is not compared.
When this bit = 1b, the current pixel value is compared with the value specified by the Compare 2 Current Pixel Value bits, REG[036Ah] bits 15-8.

REG[0368h] bit 6 Compare 2 Next Pixel Value Compare Enable
When Auto Waveform Mode is selected (REG[0330h] bit 6 = 1b), this bit determines whether the next pixel value is compared for Compare 2.
When this bit = 0b, the next pixel value is not compared.
When this bit = 1b, the next pixel value is compared with the value specified by the Compare 2 Next Pixel Value bits, REG[036Ah] bits 7-0.

REG[0368h] bits 3-0 Compare 2 Waveform Mode Number bits [3:0]
When Auto Waveform Mode is selected (REG[0330h] bit 6 = 1b), these bits specify the waveform mode number used if the pixel change is greater than or equal to the minimum threshold and the current/next pixel values are equal to the specified values (when enabled).

REG[036Ah] bits 15-8 Compare 2 Current Pixel Value bits [7:0]
When Auto Waveform Mode is selected (REG[0330h] bit 6 = 1b) and Compare 2 Current Pixel Value Compare is enabled (REG[0368h] bit 7 = 1b), these bits specify the pixel value that is compared with the current pixel value for Compare 2.

REG[036Ah] bits 7-0 Compare 2 Next Pixel Value bits [7:0]
When Auto Waveform Mode is selected (REG[0330h] bit 6 = 1b) and Compare 2 Next Pixel Value Compare is enabled (REG[0368h] bit 6 = 1b), these bits specify the pixel value that is compared with the next pixel value for Compare 2.

REG[036Ch] Auto Waveform Mode Compare 3 Configuration Register
Default = 0001h Read/Write

Reserved							
15	14	13	12	11	10	9	8
Reserved	Reserved	n/a		Compare 3 Waveform Mode Number bits 3-0			
7	6	5	4	3	2	1	0

REG[036Ch] bits 15-8 Reserved
These bits must be set to 00h.

REG[036Ch] bit 7 Reserved
This bit must be set to 0b.

REG[036Ch] bit 6 Reserved
This bit must be set to 0b.

REG[036Ch] bits 3-0 Compare 3 Waveform Mode Number bits [3:0]
When Auto Waveform Mode is selected (REG[0330h] bit 6 = 1b), these bits specify the waveform mode number used if the pixel change is greater than or equal to the minimum threshold and the current/next pixel values are equal to the specified values (when enabled).

REG[036Eh] is Reserved

This register is Reserved and should not be written.

Change Record

X88B-A-001-01 Revision 1.2 - Issued: December 09, 2008

- All changes from the previous revision are Red
- section 4.2, added note about what to do with unused pins
- section 4.2.10, added the following text to the CLKI pin description “If unused, this pin must be connected to VSS.”
- updated Revision 1.1 change record to fix reference to Waveform Modes section
- updated the International Sales Operations addresses

X88B-A-001-01 Revision 1.1 - Issued: October 09, 2008

- All changes from the previous revision are Red
- section 9.6.24, updated the description for the LD_IMG_SETADR command
- section 9.6.25, updated the description for the LD_IMG_DSPEADR command
- section 9.6.28, changed bit reference for step 1 from “REG[0338h] bit 6” to “REG[0338h] bit 5”
- section 9.6.29, changed bit reference for step 2 from “REG[0338h] bit 7” to “REG[0338h] bit 6”
- section 9.6.37, updated the bit field description for parameter 2 of the UPD_SET_IMGADR command
- section 16, updated the Waveform Modes section to clarify that the Waveform modes in the list are examples
- Appendix A, register section moved to an Appendix

X88B-A-001-01 Revision 1.0 - Issued: May 29, 2008

- created from the S1D13521B00 Spec, Rev 0.09
- All changes from the previous revision are Red
- section 2.4, 4.2.8, 18.5, REG[0020h], REG[0320h], changed references from “Dialog DA8590” to “3-wire Active Matrix Power Management IC”
- section 2.7, added comment that the Flash Memory must support the Fast Read command
- section 2.8, removed “MHz” from the clock input description
- section 3.1, in the typical system implementation diagram changed SDCE_L10 to SDOED and SDCE_L9 to SDOEX
- section 3.1, added note regarding Serial Flash requirements
- section 4.1, in the Pinout diagrams changed SDCE_L10 to SDOED and SDCE_L9 to SDOEX
- section 4.2.7, in the Pin Descriptions changed SDCE_L10 to SDOED and SDCE_L9 to SDOEX
- section 4.2.10, reworded the CNF[3:0] pin description to clarify
- section 4.3, reworded the Configuration Pins section to clarify

- section 4.3, added note for CNF2 about the timing requirements when using OSCI/OSCO
- section 4.4.2, in the Source Driver Interface table changed SDCE_L10 to SDOED and SDCE_L9 to SDOEX
- section 4.4.2, for the Source Driver Interface table clarified that SDOED and SDOEX are used for DDR only
- section 5.3, removed references to Pull-Up Resistance (Rpu) parameter for all IOVDD values
- section 6.1.1, updated Fosc max for CLKI when used as SYSCLK to 133Mhz
- section 6.2, for the Power Supply Sequence section added OSCVDD into the figures and changed the Power-On Sequence t2 min to reference the RESET_L timing section
- section 6.3, added note about example external OSC circuit and cross reference to OSC Clock Timing Requirements section
- section 6.4.1, updated Host Timing tables and figures to add the trdyrw, trwrdyl, and trdylmem parameters
- section 6.4.1, for the Host Interface Timing table, revised the min/max values and removed parameters tcodh and tcdrz
- section 6.5, removed Display Timing Register table (not needed anymore) and replaced note
- section 6.5.2, replaced the Source Driver Display Timing figures and tables
- section 6.5.3, replaced the Gate Driver Timing Generation figure and table
- section 7.1, added the OSC Enable Bypass bit to the clock tree diagram
- section 8.1, for the power management sections changed all references from “Idle” mode to “Run” mode
- section 8.1, for the Standby to Sleep transition in the State Transition Requirements table changed the command to “Run CMD SLP”
- section 9.2.1, changed “The HRDY line is deasserted (low) within 5ns...” to “The HRDY line is deasserted (low) after HWE_L is deasserted for the last parameter.”
- section 9.3, added the following note to the Serial Flash Memory Contents section “If the Serial Flash Memory is empty or contains invalid data, the RD_REG and WR_REG commands must be used to program the serial flash.”
- section 9.3, replaced the HRDY (Wait Line) Usage section
- section 9.7.2 ~ 9.7.4, changed references to power state status bits from “bits 12-10” to “bits 11-10”
- REG[0000h] bits 15-8, updated the revision code from 00h to 01h
- REG[0004h] bits 3-0, changed the CNF status bits from bits 2-0 to bits 3-0
- REG[000Ah] bit 12, added the OSC Enable Bypass bit and bit description
- REG[000Ah] bits 11-10, for the Power Save Status bits description changed reference from “Idle” mode to “Run” mode
- REG[001Ah], updated the formula for the I2C Thermal Sensor Clock Divide Ratio and updated the note
- REG[0100h] bits 14-12, changed the SDRAM Refresh Cycle Time bit description to “These bits specify the guaranteed SDRAM Refresh...” from ““These bits specify the SDRAM Refresh...”
- REG[0100h] bits 9-8, for the SDRAM Row Active Time bit description reserved option 01b, changed option 10b to 6 clocks, and changed option 11b to 7 clocks

- REG[0100h] bit 7, added the following note to the 16-bit SDRAM Enable bit description “This bit should not be changed after the SDRAM has been initialized.”
- REG[0104h] bit 8, updated the SDRAM Self Refresh Mode State bit description with a note that memory must not be accessed while SDRAM is in self refresh mode
- REG[0140h] bits 1-0, for the Memory Access Type Select bit description added a note about line data lengths greater than 2048
- REG[0144h] ~ REG[0146h], removed 256-bit boundary restriction for raw memory read starting addresses
- REG[0156h], clarified the Host Memory Checksum bit description
- REG[0158h], renamed these bits to Host Raw Memory FIFO Level, reserved bits 8-5, and changed read mode to be defined as the number of words available - 1
- REG[0204h] bit 6, added note regarding Serial Flash requirements
- REG[0220h] bits 4-0, for the 3-Wire Chip Interface Clock Divide Select bit description reserved 8:1 and 16:1 divide ratios
- REG[0240h] bit 6, REG[0242h] bit 6, REG[0244h] bit 6, updated the bit names to refer to the Host Memory Read/Write FIFO Error Interrupt and updated the bit descriptions accordingly
- REG[0240h] bit 3, updated the method used to clear the GPIO Interrupt Status bit and added references to the GPIO Interrupt Enable and GPIO Interrupt Status registers
- REG[0240h] bit 2, REG[0242h] bit 2, REG[0244h] bit 2, updated the bit names to refer to the SDRAM Access Complete Interrupt and updated the bit descriptions accordingly
- REG[0242h] bit 3, updated the method used to clear the GPIO Interrupt Masked Status bit and added references to the GPIO Interrupt Enable and GPIO Interrupt Status registers
- REG[0292h], changed the Command RAM Controller Address register from bits 11-0 to bits 10-0
- REG[0300h], for the Frame Data Length bit description added a note about line data lengths greater than 2048
- REG[0302h] bits 7-0, updated the formula for the Frame Sync Length bits
- REG[0304h] bits 15-8, updated the formula for the Frame End Length bits
- REG[0306h], for the Line Data Length bit description added a note about line data lengths greater than 2048
- REG[0306h] bits 7-0, updated the Line Data Length bit description and formulas
- REG[0308h] bits 15-8, updated the Line Sync Length bit description and formulas
- REG[030Ah] bits 15-8, updated the Line End Length bit description and formulas
- REG[030Ah] bits 7-0, updated the Line Begin Length bit description and formulas
- REG[030Ch] bits 15-12, added note 1 to the Source Driver Chip Enable Start bit description
- REG[030Ch] bit 9, added a note about 8 pixel per clock with double data rate to the Source Driver Output Reverse bit description
- REG[030Ch] bits 7-0, clarified the example for the Source Driver Output Size Select bit description
- REG[030Eh] bits 15-11, added comment that the Source Driver SDOED Delay bits are only used for 8 pixel per clock output with double data rate enabled and added note that the bits must be set greater than 0

- REG[030Eh] bit 8, reworded the Source Driver Early SDOE Assert Disable bit description
- REG[030Eh] bits 7-3, added comment that the Source Driver SDOEX Delay bits are only used for 8 pixel per clock output with double data rate enabled and added note that the bits must be set greater than 0
- REG[0326h], reserved bits 15-8 and renamed bits 7-0 to Next Border Value and clarified the bit description
- REG[0328h], reserved this register
- REG[032Ah], changed reference to the voltage control waveform format from “version 1” to “version 2”
- REG[032Ch] bits 9-8, added note that the Area Coordinate Rotation Select bits must be set the same as the Write Rotation Select bits when the Host X/Y Start/End Positions are used
- REG[032Ch] bits 5-4, reserved these bits and changed the name to Display Pipe FIFO Re-load Threshold Trigger Level
- REG[0332h], updated the Update Buffer Pixel Set Value bit description
- REG[0334h] bit 15, changed reference to the voltage control waveform format from “version 1” to “version 2”
- REG[0334h] bits 13-12, added a note to the Update Rectangle Mode bit description about performing multiple Packed Pixel Rectangular transfers when the Host X/Y Start/End positions are used
- REG[033Ah] bit 7, REG[033Ch] bit 7, REG[033Eh] bit 7, updated the bit name to “LUT Area Overlap Conflict Interrupt” from “LUT Busy Conflict Detected Interrupt”
- REG[033Ah] bit 6, REG[033Ch] bit 6, REG[033Eh] bit 6, added a note to the Display Pipe FIFO Underflow Interrupt bit descriptions that this interrupt is for debugging purposes only
- REG[0340h] ~ REG[034Eh], added notes that the X,Y Start/End coordinates must be set within the display area
- REG[0340h] ~ REG[0346h], added a note about the display engine automatic updates of these bits
- REG[0348h] ~ REG[034Eh], added comment to the Host Pixel Rectangular X/Y Start/End registers about when to read the registers and the effect of multiple packed pixel rectangular transfers
- section 13.5.2, changed reference to the “LUT Area Overlap Conflict Interrupt” from “LUT Busy Conflict Detected Interrupt”
- section 15.1, added note about the timing requirements when using OSCI/OSCO
- section 15.1.1, added Initializing and Programming a Blank Serial Flash section
- section 15.1.1, removed comment about ignoring HRDY during initial Serial Flash programming
- section 18.4.2, added a note about the SDRDAT[31:0] pins in the SDRAM Connection Example section
- section 18.4.3, updated the SDRAM Operation Timing section for the Read and Write Timing figures to correct the tRCD, tRAS, and tRP parameters
- section 19.2.1, updated the Exiting Sleep Timing Requirement for Input Clock From Oscillator figure and flow-chart to use the OSC Enable Bypass bit
- section 21, added PFBGA12UX 180-pin package mechanical drawing
- section 21, added PFBGA12UX 180-pin package marking drawing
- section 21.1, added Thermal Details for the PFBGA12UX 180-pin package

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